

# Specifications for Blanview TFT-LCD Monitor

Version 1.0

(Please be sure to check the specifications latest version. )

MODEL COM24H2P28XLC

Customer's Approval

Signature:

Name:

Section:

Title:

Date:

# ORTUSTECH

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## 1. Application

This Specification is applicable to 6.00cm (2.4 inch) Blanview TFT-LCD monitor for non-military use.

- ◎ ORTUS TECHNOLOGY makes no warranty or assume no liability that use of this Product and/or any information including drawings in this Specification by Purchaser is not infringing any patent or other intellectual property rights owned by third parties, and ORTUS TECHNOLOGY shall not grant to Purchaser any right to use any patent or other intellectual property rights owned by third parties. Since this Specification contains ORTUS TECHNOLOGY's confidential information and copy right, Purchaser shall use them with high degree of care to prevent any unauthorized use, disclosure, duplication, publication or dissemination of ORTUS TECHNOLOGY'S confidential information and copy right.
- ◎ If Purchaser intends to use this Products for an application which requires higher level of reliability and/or safety in functionality and/or accuracy such as transport equipment (aircraft, train, automobile, etc.), disaster-prevention/security equipment or various safety equipment, Purchaser shall consult ORTUS TECHNOLOGY on such use in advance.
- ◎ This Product shall not be used for application which requires extremely higher level of reliability and/or safety such as aerospace equipment, telecommunication equipment for trunk lines, control equipment for nuclear facilities or life-support medical equipment.
- ◎ It must be noted as a mechanical design manner, especial attention in housing design to prevent arcuation/flexure or caused by stress to the LCD module shall be considered.
- ◎ ORTUS TECHNOLOGY assumes no liability for any damage resulting from misuse, abuse, and/or miss-operation of the Product deviating from the operating conditions and precautions described in the Specification.
- ◎ ORTUS TECHNOLOGY is not responsible for any nonconformities and defects that are not specified in this specifications.
- ◎ If any issue arises as to information provided in this Specification or any other information, ORTUS TECHNOLOGY and Purchaser shall discuss them in good faith and seek solution.
- ◎ ORTUS TECHNOLOGY assumes no liability for defects such as electrostatic discharge failure occurred during peeling off the protective film or Purchaser's assembly process.
- ◎ This Product is compatible for RoHS directive.

Object substance	Maximum content [ppm]
Cadmium and its compound	100
Hexavalent Chromium Compound	1000
Lead & Lead compound	1000
Mercury & Mercury compound	1000
Polybrominated biphenyl series (PBB series)	1000
Polybrominated biphenyl ether series (PBDE series)	1000

## 2. Outline Specifications

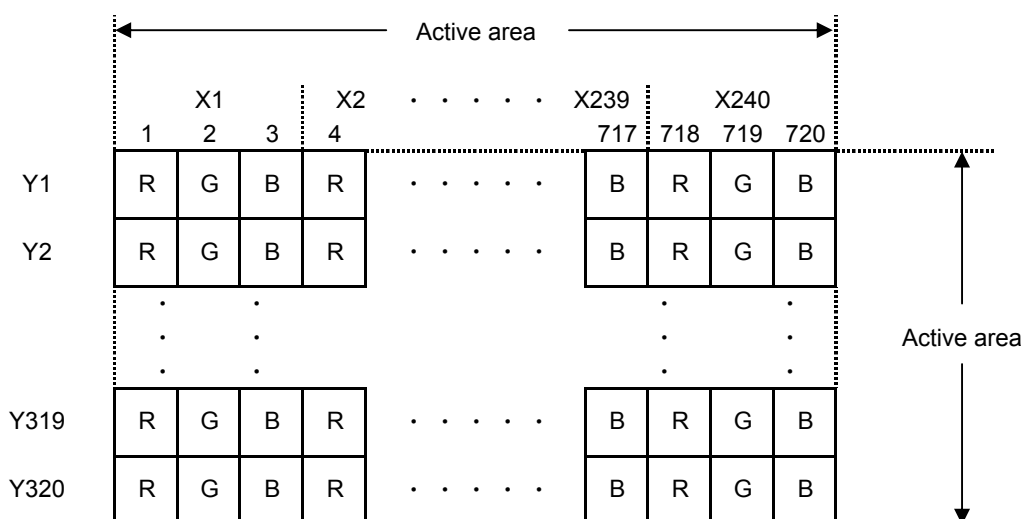
### 2.1 Features of the Product

- 2.4 inch diagonal display, 720 [H] x 320 [V] dots.
- 6-bit / 262,144 colors.
- 2.7V voltage single power source.
- Timing generator [TG], Counter-electrode driving circuitry, Built-in power supply circuit.
- Long life & High bright white LED back-light.
- Blanview TFT-LCD, improved outdoor readability.

	Indoor		Outdoor	
	Readability	Power Efficiency (Battery Life)	Readability	Power Efficiency (Battery Life)
Transmissive	Good	Good	Fair	Poor
Transflective	Fair	Poor	Good	Good
Blanview	Good	Good	Good	Good

### 2.2 Display Method

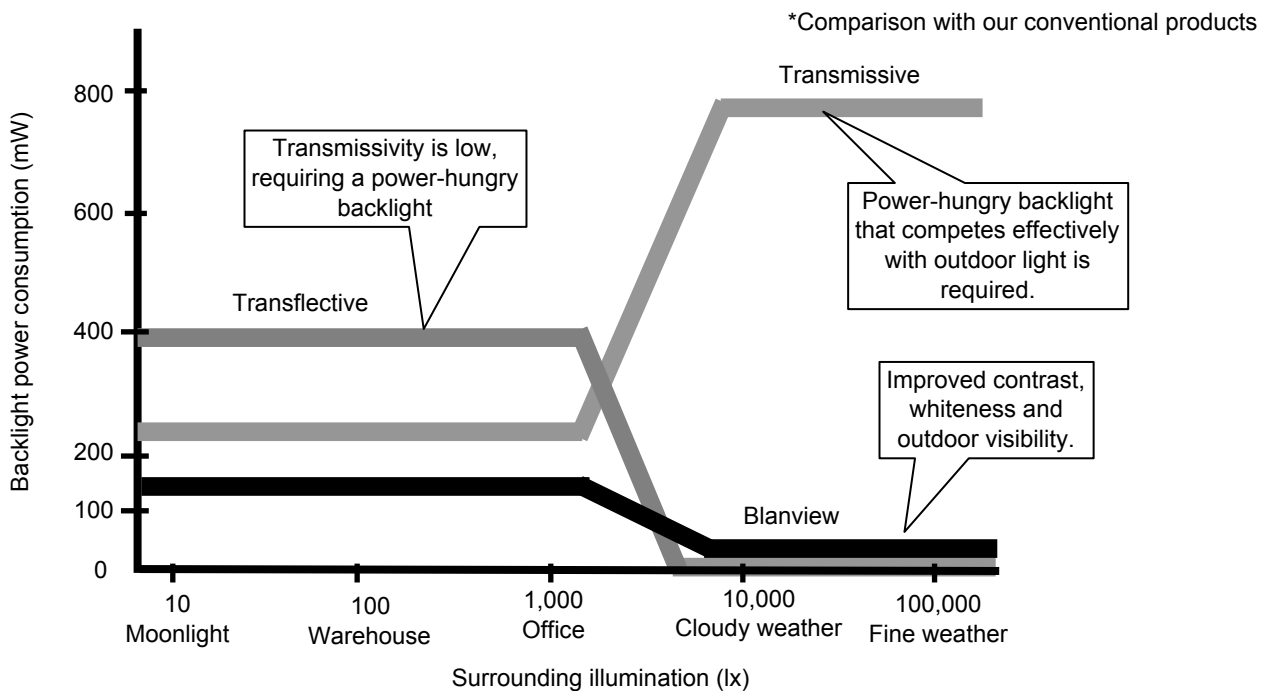
Items	Specifications	Remarks
Display type	TN type 262,144 colors. Blanview, Normally white.	
Driving method	a-Si TFT Active matrix. Line-scanning, Non-interlace.	
Dot arrangement	RGB stripe arrangement.	Refer to "Dot arrangement"
Signal input method	6-bit RGB, parallel input.	
Backlight type	Long life & High bright white LED.	



Dot arrangement (FPC cable placed left)

<Features of Blanview>

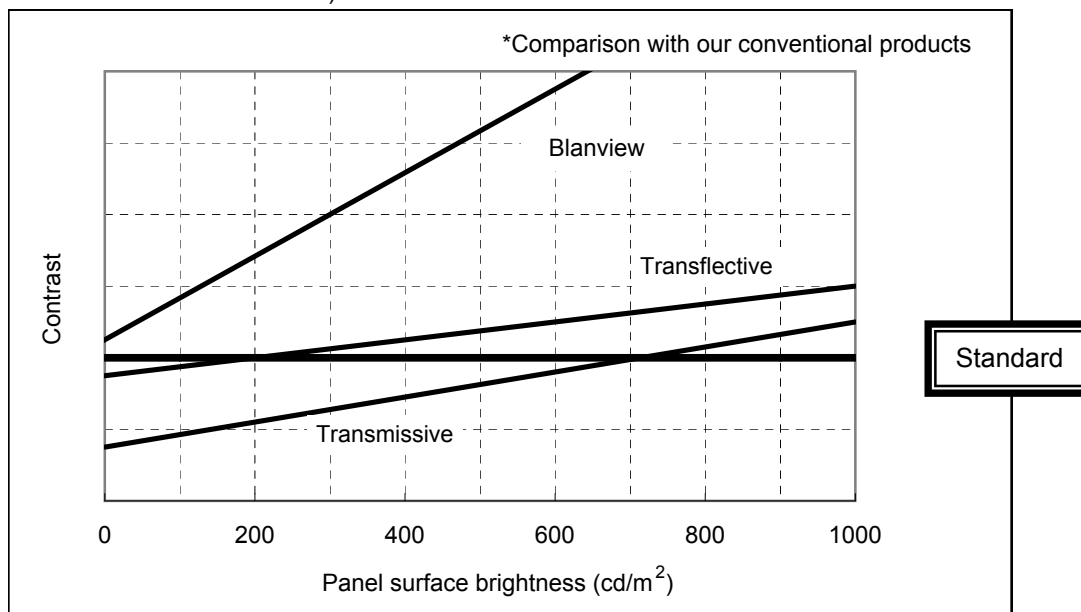
- Backlight power consumption required to assure visibility. (equivalent to 3.5"QVGA )



- Contrast characteristics under 100,000lx. (same condition as direct sunlight.)

With better contrast (higher contrast ratio), Blanview TFT-LCD has the best outdoor readability in three different types of TFT-LCD.

Below chart shows contrast value against panel surface brightness. (Horizontal: Panel surface brightness/ Vertical: Contrast value) LCD panel has enough outdoor readability above our Standard line. (ORTUS TECHNOLOGY criteria)



## 3. Dimensions and Shape

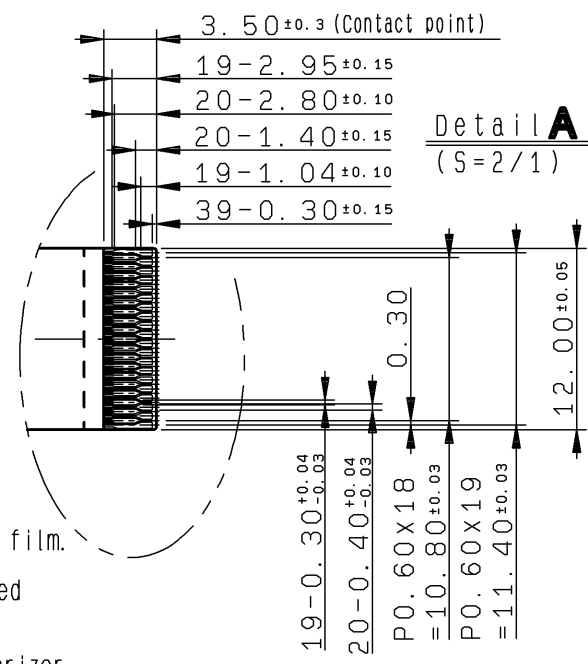
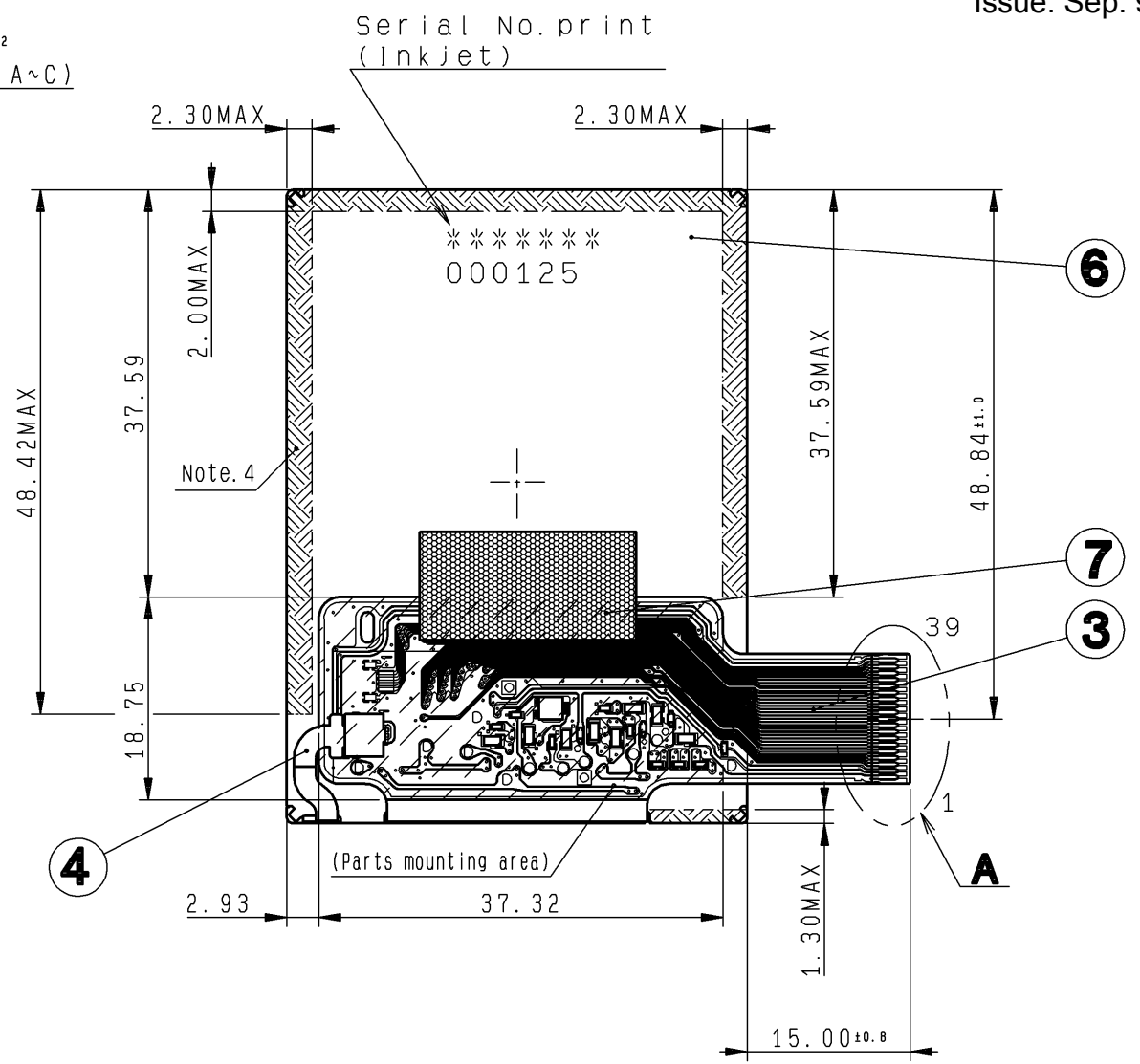
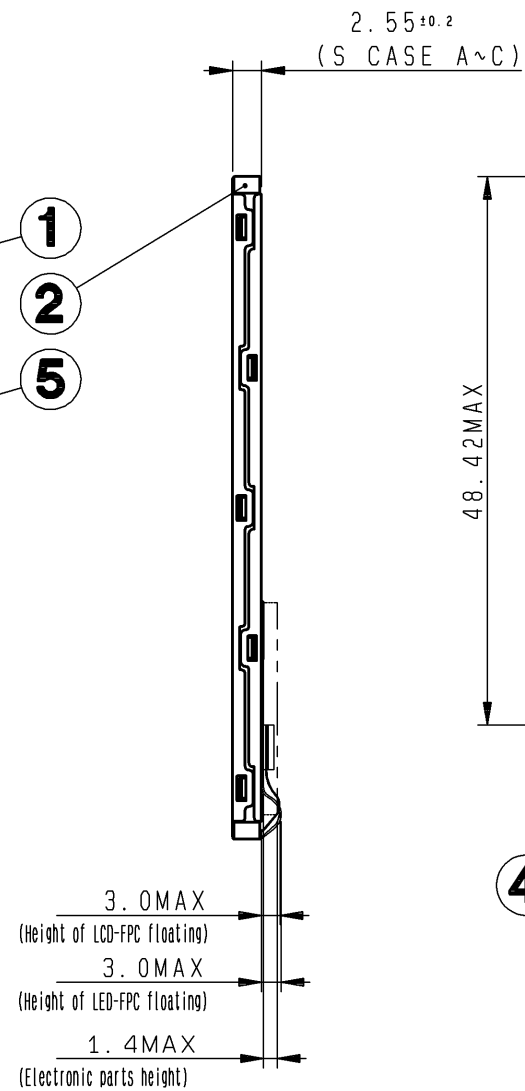
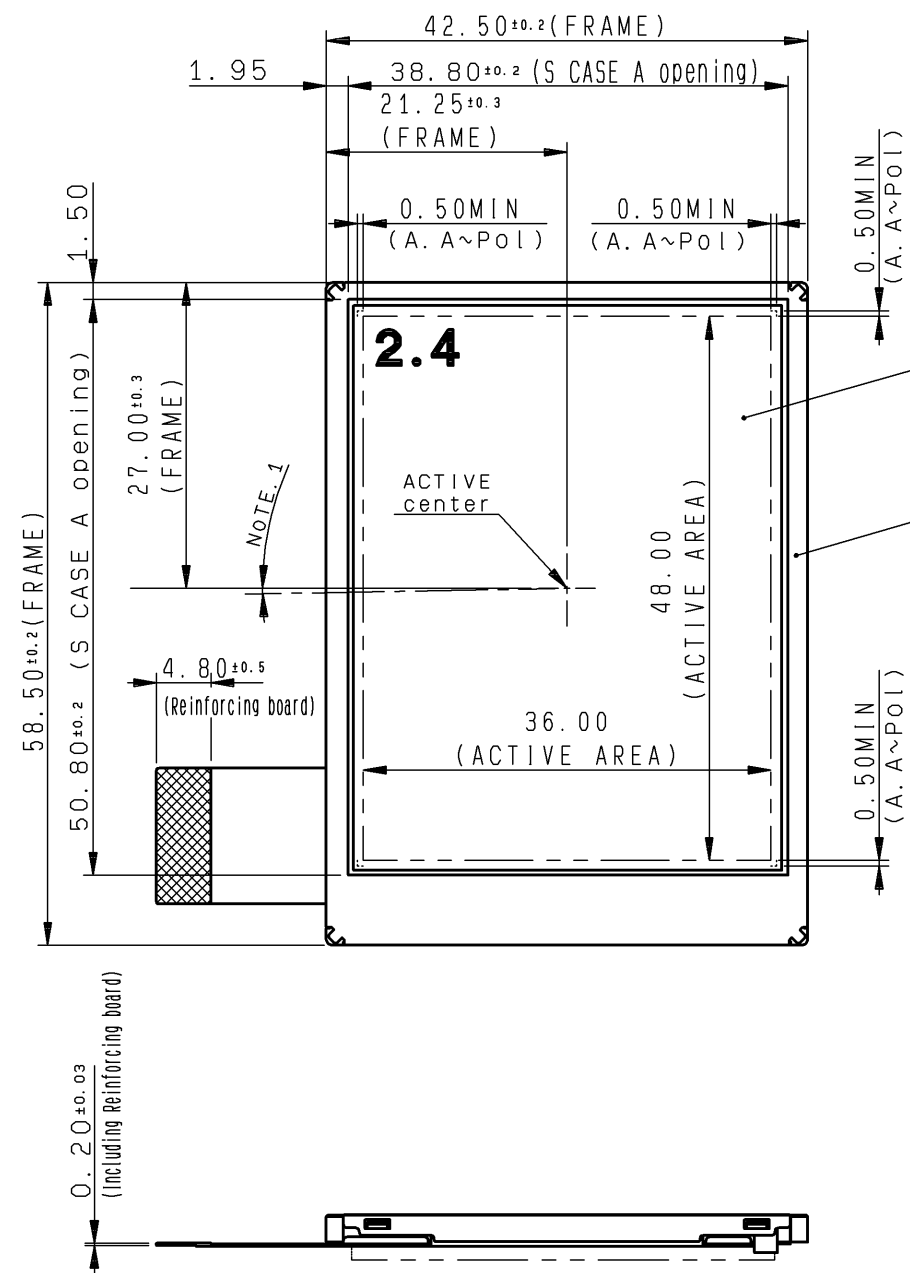
## 3.1 Dimensions

Items	Specifications	Unit	Remarks
Outline dimensions	42.50[H] × 58.50[V] × 2.60[D]	mm	Exclude FPC cable and parts on FPC.
Active area	36.00[H] × 48.00[V]	mm	6.00cm diagonal
Number of dots	720[H] × 320[V]	dot	
Dot pitch	50.0[H] × 150.0[V]	μm	
Surface hardness of the polarizer	3	H	Load:2.0N
Weight	13.6	g	Include FPC cable

EC No.	REV. No.	REVISE	DATE (Y:M:D)	APPROVED	CHECKED	PREPARED
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3.2 Outward Form

(8/41)  
14TLM133  
Issue: Sep. 9, 2015



- Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than  $[\pm 40']$ .
- Note 2. Recommended FPC connectors  
For LCD : HIROSE, part number: FH23-39S-0.3SHW(05) (Lower Contact)
- Note 3. Protective film is affixed on front surface of the screen.  
Location tolerance of the protective film shall be  $\pm 1.5$  mm to the polarizing film.
- Note 4. In case TFT-LCD monitor is fixed to the case of your product, it's recommended that monitor is fixed in to area.
- Note 5. Refer to "13.CRITERIA OF JUDGMENT" about the appearance specification of a polarizer.

	8			
I-TAPE	7			
S CASE C	6			
S CASE A	5			
LED-FPC	4			
LCD-FPC	3			
FRAME	2		PC	
LCD	1		Glass substrate thickness=0.5t	
PART NAME	ITEM	PART CODE	MATERIAL GRADE	REMARK

APPROVED 橋爪	GENERAL TOLERANCE $\pm 0.5$	SCALE FREE (2/1)	UNIT mm	<b>ORTUSTECH</b> ORTUS TECHNOLOGY CO., LTD. DO NOT DUPLICATE. CONFIDENTIAL AND PROPRIETARY		
CHECKED 平信	ISSUE (Y:M:D) 15:08:11	MODEL CCM24H2P28X**				
CHECKED	NAME	<b>OUTLINE-D2P28</b>		DRAWING No. RJD527410D301		
DESIGN 渡辺				REV.	SHEET	DIV.
DRAW 渡辺						



## 3.3 Serial No. print (S-print)

## 1) Display Items

S-print indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (5characters), serial number (6digits).

## \* Contents of Display

*	*	*****	*****
-	-	-----	-----
a	b	c	d

	Contents of display			
a	The least significant digit of manufacture year			
b	Manufacture month	Jan-A Feb-B Mar-C Apr-D	May-E Jun-F Jul-G Aug-H	Sep-I Oct-J Nov-K Dec-L
c	Model code	24AZC (Made in Japan) 24BAC (Made in Malaysia)		
d	Serial number			

## \* Example of indication of Serial No. print (S-print)

## •Made in Japan

6J24AZC000125

means "manufactured in October 2016, 2.4" AZ type, C specifications, serial number 000125"

## •Made in Malaysia

6J24BAC000125

means "manufactured in October 2016, 2.4" BA type, C specifications, serial number 000125"

## 2) Location of Serial No. print (S-print)

Refer to 3.2 "Outward Form".

## 3)Others

Please note that it is likely to disappear with an organic solvent about the Serial print.

## 4. Pin Assignment

No.	Symbol	Function
1	VSS	GND.
2	VSS	GND.
3	VCI	Power supply.
4	IOVCC	Power supply.
5	VSS	GND.
6	RESETB	Reset signal.(Lo: active)
7	CSB	Chip select signal.(Lo: Selected,Hi: Not selected)
8	RS	Select the register signal.(Lo:Index,Hi:command or display data)
9	WRB	Write strobe Signal.
10	VSS	GND.
11	D0	Data Input & Output.
12	D1	Data Input & Output.
13	D2	Data Input & Output.
14	D3	Data Input & Output.
15	D4	Data Input & Output.
16	D5	Data Input & Output.
17	D6	Data Input & Output.
18	D7	Data Input & Output.
19	D8	Data Input & Output.
20	D9	Data Input & Output.
21	D10	Data Input & Output.
22	D11	Data Input & Output.
23	D12	Data Input & Output.
24	D13	Data Input & Output.
25	D14	Data Input & Output.
26	D15	Data Input & Output.
27	D16	Data Input & Output.(Please connect it with VSS when 16bit interface.)
28	D17	Data Input & Output.(Please connect it with VSS when 16bit interface.)
29	VSS	GND.
30	BS0	Select interface mode.
31	BS1	Select interface mode.
32	RDB	Read strobe signal.(Please connect it with IOVCC when not in use.)
33	NC	OPEN.
34	NC	OPEN.
35	NC	OPEN.
36	NC	OPEN.
37	TE	Frame head output pulse.(Please open this pin when not in use.)
38	BLH	LED drive power source. (Anode side)
39	BLL	LED drive power source. (Cathode side)

- Recommended connector : HIROSE ELECTRIC CO.,LTD. FH23 series [FH23-51S-0.3SHW(05)]
- Please make sure to check a consistency between pin assignment in "3.2 Outward Form" and your connector pin assignment when designing your circuit.  
Inconsistency in input signal assignment may cause a malfunction.
- Since FPC cable has gold plated terminals, gilt finish contact shoe connector is recommended.
- The interface mode setting terminal is fixed on FPC as follows.  
BS2 = VSS

## 5. Absolute Maximum Rating

VSS=0V

Item	Symbol	Condition	Rating		Unit	Applicable terminal
			MIN	MAX		
Supply voltage	VCI	Ta=25 °C	-0.3	4.6	V	VCI
Supply logic interface voltage	IOVCC		-0.3	VCI	V	IOVCC
Input voltage for logic	VI		-0.3	IOVCC+0.3	V	RESETB,CSB,RS,WRB D0-D17,BS0,BS1,RDB
LED forward current	IL	Ta = 25 °C	--	35	mA	BLH - BLL
		Ta = 70 °C	--	15		
Storage temperature range	Tstg		-30	80	°C	
Storage humidity range	Hstg	Non condensing in an environmental moisture at or less than 40 °C90%RH.				

## 6. Recommended Operating Conditions

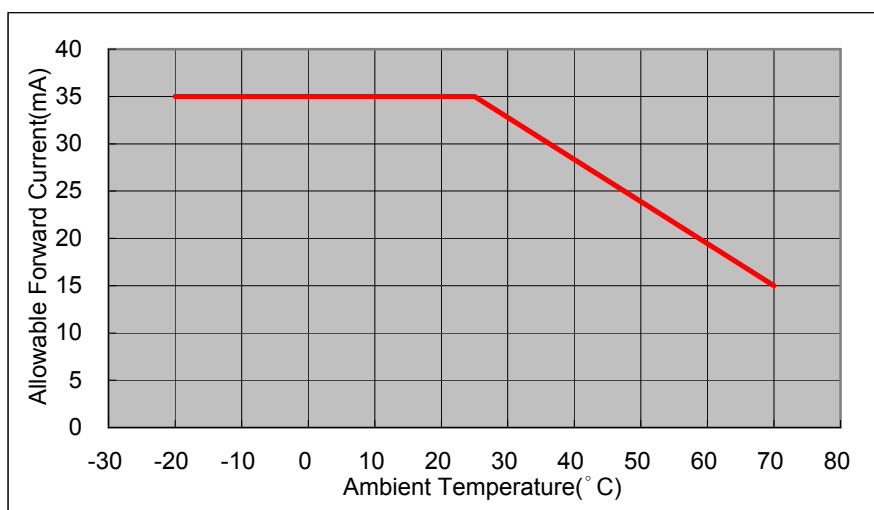
VSS=0V

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Supply voltage	VCI	Ta=25 °C	2.6	2.7	3.6	V	VCI
Supply voltage	IOVCC		1.65	VCI	VCI	V	IOVCC
Input voltage for logic	VI		0	--	IOVCC	V	RESETB,CSB,RS,WRB D0-D17,BS0,BS1,RDB
Operational temperature range	Top	Note1,2	-20	25	70	°C	Panel surface temperature
Operating humidity range	Hop	Ta ≤ 30 °C	20	--	80	%	
		Ta > 30 °C	Non condensing in an environmental moisture at or less than 30 °C80%RH.				

Note1: This monitor is operatable in this temperature range. With regard to optical characteristics, refer to Item 12."CHARACTERISTICS".

Note 2: Acceptable Forward Current to LED is up to 15mA, when Ta=+70 °C.

Do not exceed Allowable Forward Current shown on the chart below.



## 7. Characteristics

## 7.1 DC Characteristics

## 7.1.1 Display Module

(Unless otherwise noted, Ta=25°C, VCI=2.7V, IOVCC=2.7V, VSS=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Input Signal Voltage	VIH		0.7×IOVCC	--	IOVCC	V	RESETB,CSB,RS,WRB
	VIL		0	--	0.3×IOVCC	V	D0-D17,BS0,BS1,RDB
Output Signal Voltage	VOH	IOH=-0.1mA	0.8×IOVCC	--	--	V	D0-D17,TE
	VOL	IOL=0.1mA	--	--	0.2×IOVCC	V	
Operating Current	ICI	Color bar display	--	5.5	11.0	mA	VCI
	IOICC	Still image Note	--	0.5	1.0	μA	IOVCC
Standby Current	ICIs	Other input with constant voltage	--	1.0	2.0	μA	VCI
	IOICCs		--	6.0	25.0	μA	IOVCC

Note: A still image (color bar) on display , when CPU dose not access to GRAM .

## 7.1.2 Backlight

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Forward current	IL25	Ta=25°C	—	7.5	35.0	mA	BLH - BLL
	IL70	Ta=70°C	—	—	15.0	mA	
Forward voltage	VL	Ta=25°C, IL=7.5mA	—	5.4	5.6	V	
Estimated Life of LED	LL	Ta=25°C, IL=7.5mA Note	—	(50,000)	—	hr	

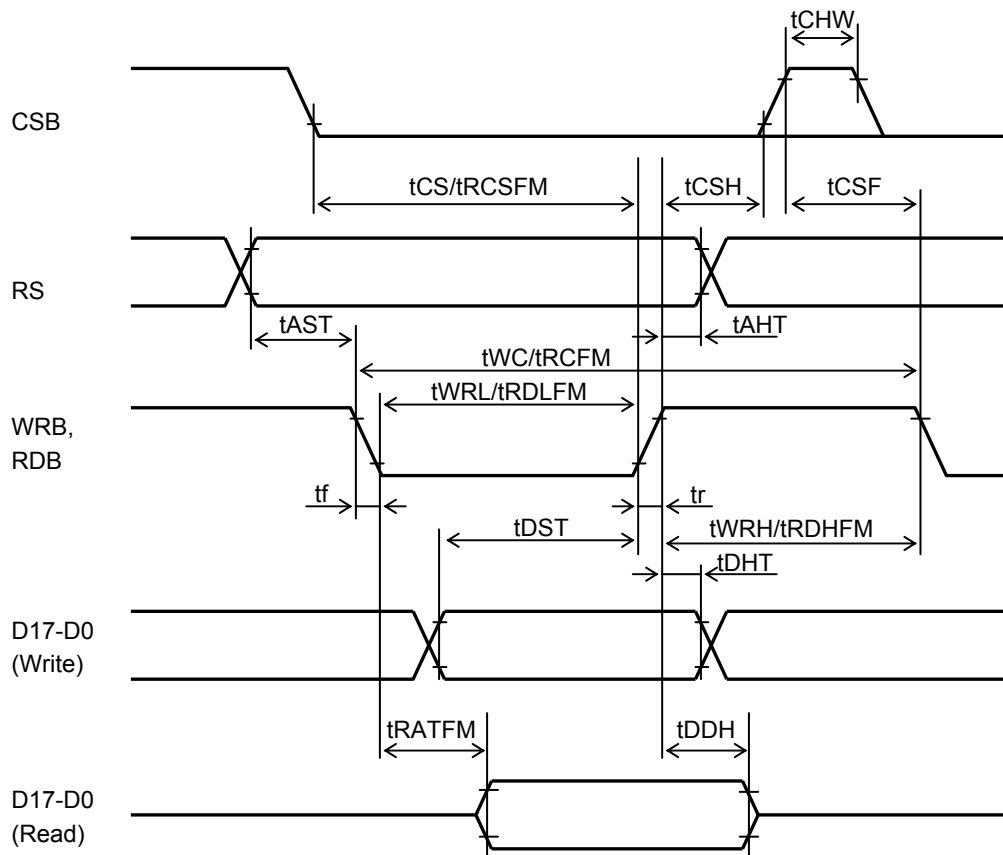
- Note: - The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not as a guarantee.
  - This figure is estimated for an LED operating alone.
- As the performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

## 7.2 AC Characteristics

(Unless otherwise noted,  $T_a=25^\circ\text{C}$ ,  $V_{CI}=2.7\text{V}$ ,  $\text{IOVCC}=2.7\text{V}$ ,  $V_{SS}=0\text{V}$ )

Item	Symbol	Condition	Rating		Unit
			MIN	MAX	
Address setup time	$t_{AST}$	RS	10	-	ns
Address hold time	$t_{AHT}$	RS	10	-	ns
CSB high level pulse width	$t_{CHW}$	CSB	0	-	ns
CSB setup time	$t_{CS}$	CSB-WRB	35	-	ns
	$t_{RCSFM}$	CSB-RDB	180	-	ns
CSB wait time	$t_{CSF}$	CSB	10	-	ns
CSB hold time	$t_{CSH}$	CSB	10	-	ns
WRB bus cycle time	$t_{WC}$	WRB	100	-	ns
WRB high level pulse width	$t_{WRH}$	WRB	15	-	ns
WRB low level pulse width	$t_{WRL}$	WRB	20	-	ns
RDB bus cycle time	$t_{RCFM}$	WRB	250	-	ns
RDB high level pulse width	$t_{RDHFM}$	WRB	15	-	ns
RDB low level pulse width	$t_{RDLFM}$	WRB	180	-	ns
WRB data setup time	$t_{DST}$	D17-D0	10	-	ns
WRB data hold time	$t_{DHT}$	D17-D0	10	-	ns
RDB access time	$t_{RATFM}$	D17-D0	-	340	ns
RDB Output disable time	$t_{DDH}$	D17-D0	20	80	ns
Input signal rising time	$t_r$		-	15	ns
Input signal falling time	$t_f$		-	15	ns

- The switching voltage is set at 30% to 70% of IOVCC voltage .



8. Interface

Bus Width	Index/ Command Write	GRAM Write			
Transferring Method		CPU			
Width of data of 1 pixel		18bit	16bit	16bit	8bit
BS1	*	18	16	16+2	6+6+6
BS0	*	18	16	18	18
		H	L	L	H
		L	L	H	H

D17																		
D16																		
D15																		
D14																		
D13																		
D12																		
D11																		
D10																		
D9																		
D8																		
D7	ID7	RB7																
D6	ID6	RB6																
D5	ID5	RB5																
D4	ID4	RB4																
D3	ID3	RB3																
D2	ID2	RB2																
D1	ID1	RB1																
D0	ID0	RB0																

R5																		
R4																		
R3	R5/R0	R5																
R2	R4	R4																
R1	R3	R3																
R0	R2	R2																
G5	R1	R1																
G4	G5	R0																
G3	G4	G5																
G2	G3	G4																
G1	G2	G3																
G0	G1	G2																
B5	G0	G1																
B4	B5/B0	G0																
B3	B4	B5																
B2	B3	B4																
B1	B2	B3	B1															
B0	B1	B2	B0															

- Please connect an unused terminal of D0-D17 with VSS.

## 9. Register List

Register	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
R01h	Display Mode control	*	*	*	*	*	IDMON	INVON	NORON	PTLON
	initial (0006h)					0	1	1	0	
	recommend (0006h)					0	1	1	0	
R02h	Column address start 2	*	SC[15:8]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R03h	Column address start 1	*	SC[7:0]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R04h	Column address end 2	*	EC[15:8]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R05h	Column address end 1	*	EC[7:0]							
	initial (00EFh)		1	1	1	0	1	1	1	
	recommend (00EFh)		1	1	1	0	1	1	1	
R06h	Row address start 2	*	SP[15:8]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R07h	Row address start 1	*	SP[7:0]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R08h	Row address end 2	*	EP[15:8]							
	initial (0001h)		0	0	0	0	0	0	1	
	recommend (0001h)		0	0	0	0	0	0	1	
R09h	Row address end 1	*	EP[7:0]							
	initial (003Fh)		0	0	1	1	1	1	1	
	recommend (003Fh)		0	0	1	1	1	1	1	
R0Ah	Partial area start row 2	*	PSL[15:8]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R0Bh	Partial area start row 1	*	PSL[7:0]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R0Ch	Partial area end row 2	*	PEL[15:8]							
	initial (0001h)		0	0	0	0	0	0	1	
	recommend (0001h)		0	0	0	0	0	0	1	
R0Dh	Partial area end row 1	*	PEL[7:0]							
	initial (003Fh)		0	0	1	1	1	1	1	
	recommend (003Fh)		0	0	1	1	1	1	1	
R0Eh	Vertical Scroll Top fixed area 2	*	TFA[15:8]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R0Fh	Vertical Scroll Top fixed area 1	*	TFA[7:0]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	
R10h	Vertical Scroll height area 2	*	VSA[15:8]							
	initial (0001h)		0	0	0	0	0	0	1	
	recommend (0001h)		0	0	0	0	0	0	1	
R11h	Vertical Scroll height area 1	*	VSA[7:0]							
	initial (0040h)		0	1	0	0	0	0	0	
	recommend (0040h)		0	1	0	0	0	0	0	
R12h	Vertical Scroll Button area 2	*	BFA[15:8]							
	initial (0000h)		0	0	0	0	0	0	0	
	recommend (0000h)		0	0	0	0	0	0	0	

Register		D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R13h	Vertical Scroll Button area 1	*	BFA[7:0]							
	initial	(0000h)	0	0	0	0	0	0	0	0
	recommend	(0000h)	0	0	0	0	0	0	0	0
R14h	Vertical Scroll Start address 2	*	VSP[15:8]							
	initial	(0000h)	0	0	0	0	0	0	0	0
	recommend	(0000h)	0	0	0	0	0	0	0	0
R15h	Vertical Scroll Start address 1	*	VSP[7:0]							
	initial	(0000h)	0	0	0	0	0	0	0	0
	recommend	(0000h)	0	0	0	0	0	0	0	0
R16h	Memory Access control	*	MY	MX	MV	*	BGR	*	*	*
	initial	(0000h)	0	0	0		0			
	recommend	(0008h)	0	0	0		1			
R18h	Gate Scan control	*	*	*	*	*	*	*	SCROL L_ON	SM
	initial	(0000h)							0	0
	recommend	(0001h)							0	1
R19h	OSC Control 1	*	CADJ[3:0]				CUADJ[2:0]			OSC_ EN
	initial	(0086h)	1	0	0	0	0	1	1	0
	recommend	(0087h)	1	0	0	0	0	1	1	1
R1Ah	OSC Control 2	*	*	*	*	*	*	*	*	OSC_ TEST
	initial	(0000h)								0
	recommend	(0000h)								0
R1Bh	Power Control 1	*	GAS ENB	*	*	PON	DK	XDK	VLCD_ TRI	STB
	initial	(0000h)	0			0	0	0	0	0
	recommend	(0014h)	0			1	0	1	0	0
R1Ch	Power Control 2	*	*	*	*	*	*	AP[2:0]		
	initial	(0004h)						1	0	0
	recommend	(0004h)						1	0	0
R1Dh	Power Control 3	*	*	*	*	*	*	VC1[2:0]		
	initial	(0004h)						1	0	0
	recommend	(0005h)						1	0	1
R1Eh	Power Control 4	*	*	*	*	*	*	VC3[2:0]		
	initial	(0000h)						0	0	0
	recommend	(0000h)						0	0	0
R1Fh	Power Control 5	*	*	*	*	*	VRH[3:0]			
	initial	(0006h)					0	1	1	0
	recommend	(0007h)					0	1	1	1
R20h	Power Control 6	*	BT[3:0]				*	*	*	*
	initial	(0060h)	0	1	1	0				
	recommend	(0000h)	0	0	0	0				
R21h	Power Control 7	*	*	*	FS1[1:0]		*	*	FS0[1:0]	
	initial	(0010h)			0	1			0	0
	recommend	(0010h)			0	1			0	0
R22h	Write Data		GRAM Write							
	initial	(0000h)								
	recommend	(0000h)								
R23h	Cycle Control 1	*	N_DC[7:0]							
	initial	(0095h)	1	0	0	1	0	1	0	1
	recommend	(0095h)	1	0	0	1	0	1	0	1
R24h	Cycle Control 2	*	PI_DC[7:0]							
	initial	(0095h)	1	0	0	1	0	1	0	1
	recommend	(0095h)	1	0	0	1	0	1	0	1



Register		D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R25h	Cycle Control 3	*	I_DC[7:0]							
	initial	(00FFh)	1	1	1	1	1	1	1	1
	recommend	(00FFh)	1	1	1	1	1	1	1	1
R26h	Display Control 1	*	PT[1:0]		GON	DTE	D[1:0]		*	*
	initial	(00A0h)	1	0	1	0	0	0		
	recommend	(00BCh)	1	0	1	1	1	1		
R27h	Display Control 2	*	*	*	*	*	N_BP[3:0]			
	initial	(0002h)					0	0	1	0
	recommend	(0002h)					0	0	1	0
R28h	Display Control 3	*	*	*	*	*	N_FP[3:0]			
	initial	(0002h)					0	0	1	0
	recommend	(0003h)					0	0	1	1
R29h	Display Control 4	*	*	*	*	*	PI_BP[3:0]			
	initial	(0002h)					0	0	1	0
	recommend	(0008h)					1	0	0	0
R2Ah	Display Control 5	*	*	*	*	*	PI_FP[3:0]			
	initial	(0002h)					0	0	1	0
	recommend	(0008h)					1	0	0	0
R2Bh	Power Control 11	*	*	*	PI_PRE_REFRESH[1:0]		BLANK_DIV[3:0]			
	initial	(0000h)			0	0	0	0	0	0
	recommend	(0000h)			0	0	0	0	0	0
R2Ch	Display Control 6	*	*	*	*	*	I_BP[3:0]			
	initial	(0002h)					0	0	1	0
	recommend	(0008h)					1	0	0	0
R2Dh	Display Control 7	*	*	*	*	*	I_FP[3:0]			
	initial	(0002h)					0	0	1	0
	recommend	(0008h)					1	0	0	0
R35h	Display Control 9	*	EQS[7:0]							
	initial	(0009h)	0	0	0	0	1	0	0	1
	recommend	(0009h)	0	0	0	0	1	0	0	1
R36h	Display Control 10	*	EQP[7:0]							
	initial	(0009h)	0	0	0	0	1	0	0	1
	recommend	(0009h)	0	0	0	0	1	0	0	1
R37h	Display Control 12	*	*	*	PTG[1:0]		ISC[3:0]			
	initial	(0000h)			0	0	0	0	0	0
	recommend	(0000h)			0	0	0	0	0	0
R38h	RGB interface control 1	*	*	*	*	RGB_EN	DPL	HSPL	VSPL	EPL
	initial	(0000h)				0	0	0	0	0
	recommend	(0000h)				0	0	0	0	0
R39h	RGB interface control 2	*	DOTCLK_DIV[7:0]							
	initial	(0000h)	0	0	0	0	0	0	0	0
	recommend	(0000h)	0	0	0	0	0	0	0	0
R3Ah	Cycle Control 1	*	N_RTN[3:0]			*	N_NW[2:0]			
	initial	(0001h)	0	0	0	0		0	0	1
	recommend	(00A1h)	1	0	1	0		0	0	1
R3Bh	Cycle Control 2	*	PI_RTN[3:0]			*	PI_NW[2:0]			
	initial	(0001h)	0	0	0	0		0	0	1
	recommend	(00A1h)	1	0	1	0		0	0	1
R3Ch	Cycle Control 3	*	I_RTN[3:0]			*	I_NW[2:0]			
	initial	(00F0h)	1	1	1	1		0	0	0
	recommend	(00A0h)	1	0	1	0		0	0	0

Register		D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R3Dh	Cycle Control 4	*	*	*	DIV_I[1:0]		DIV_PI[1:0]		DIV_N[1:0]	
	initial	(0000h)			0	0	0	0	0	0
	recommend	(0000h)			0	0	0	0	0	0
R3Eh	Cycle Control 5	*	SON[7:0]							
	initial	(0038h)	0	0	1	1	1	0	0	0
	recommend	(002Dh)	0	0	1	0	1	1	0	1
R40h	Cycle Control 6	*	GDON[7:0]							
	initial	(0003h)	0	0	0	0	0	0	1	1
	recommend	(0003h)	0	0	0	0	0	0	1	1
R41h	Cycle Control 7	*	GDOF[7:0]							
	initial	(00F8h)	1	1	1	1	1	0	0	0
	recommend	(00CCh)	1	1	0	0	1	1	0	0
R42h	BGP Control	*	*	*	*	VBGP_OE	BGP[3:0]			
	initial	(0008h)				0	1	0	0	0
	recommend	(0008h)				0	1	0	0	0
R43h	VCOM Control 1	*	VCOMG	*	*	*	*	*	*	*
	initial	(0080h)	1							
	recommend	(0080h)	1							
R44h	VCOM Control 2	*	*	VCM[6:0]						
	initial	(005Ah)		1	0	1	1	0	1	0
	recommend	(007Fh)		1	1	1	1	1	1	1
R45h	VCOM Control 3	*	*	*	*	VDV[4:0]				
	initial	(0011h)				1	0	0	0	1
	recommend	(0014h)				1	0	1	0	0
R46h	r Control 1	*	GSEL	CP1[2:0]		*	CP0[2:0]			
	initial	(0000h)	0	0	0		0	0	0	
	recommend	(0086h)	1	0	0		1	1	0	
R47h	r Control 2	*	*	CN1[2:0]		*	CN0[2:0]			
	initial	(0000h)		0	0	0	0	0	0	
	recommend	(0060h)		1	1	0	0	0	0	
R48h	r Control 3	*	*	NP1[2:0]		*	NP0[2:0]			
	initial	(0000h)		0	0	0	0	0	0	
	recommend	(0001h)		0	0	0	0	0	1	
R49h	r Control 4	*	*	NP3[2:0]		*	NP2[2:0]			
	initial	(0000h)		0	0	0	0	0	0	
	recommend	(0067h)		1	1	0	1	1	1	
R4Ah	r Control 5	*	*	NP5[2:0]		*	NP4[2:0]			
	initial	(0000h)		0	0	0	0	0	0	
	recommend	(0046h)		1	0	0	1	1	0	
R4Bh	r Control 6	*	*	NN1[2:0]		*	NN0[2:0]			
	initial	(0000h)		0	0	0	0	0	0	
	recommend	(0013h)		0	0	1	0	1	1	
R4Ch	r Control 7	*	*	NN3[2:0]		*	NN2[2:0]			
	initial	(0000h)		0	0	0	0	0	0	
	recommend	(0001h)		0	0	0	0	0	1	
R4Dh	r Control 8	*	*	NN5[2:0]		*	NN4[2:0]			
	initial	(0000h)		0	0	0	0	0	0	
	recommend	(0067h)		1	1	0	1	1	1	
R4Eh	r Control 9	*	CGMP1[1:0]		CGMP0[1:0]		OP0[3:0]			
	initial	(0000h)	0	0	0	0	0	0	0	
	recommend	(0000h)	0	0	0	0	0	0	0	

Register		D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R4Fh	r Control 10	*	CGMP3	CGMP2	*	OP1[4:0]				
	initial (0000h)		0	0	0	0	0	0	0	0
	recommend (0013h)		0	0	0	1	0	0	1	1
R50h	r Control 11	*	CGMN1[1:0]		CGMN0[1:0]		ON0[3:0]			
	initial (0000h)		0	0	0	0	0	0	0	0
	recommend (0002h)		0	0	0	0	0	0	1	0
R51h	r Control 12	*	CGMN3	CGMN2	*	ON1[4:0]				
	initial (0000h)		0	0	0	0	0	0	0	0
	recommend (0000h)		0	0	0	0	0	0	0	0
R52h	OTP Control 1	*	OTP_MASK[7:0]							
	initial (0000h)		0	0	0	0	0	0	0	0
	recommend (0000h)		0	0	0	0	0	0	0	0
R53h	OTP Control 2	*	OTP_INDEX[7:0]							
	initial (00FFh)		1	1	1	1	1	1	1	1
	recommend (00FFh)		1	1	1	1	1	1	1	1
R54h	OTP Control 3	*	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_PTM	0	VPP_SEL	OTP_PROG
	initial (0008h)		0	0	0	0	1		0	0
	recommend (0008h)		0	0	0	0	1		0	0
R64h	Internal Use 16	*	ID1[7:0]							
	initial (0000h)		0	0	0	0	0	0	0	0
	recommend (0000h)		0	0	0	0	0	0	0	0
R65h	Internal Use 17	*	*	ID2[6:0]						
	initial (0000h)			0	0	0	0	0	0	0
	recommend (0000h)			0	0	0	0	0	0	0
R66h	Internal Use 18	*	ID3[7:0]							
	initial (0000h)		0	0	0	0	0	0	0	0
	recommend (0000h)		0	0	0	0	0	0	0	0
R67h	Internal Use 19	*	ID4[7:0]							
	initial (0047h)		0	1	0	0	0	1	1	1
	recommend (0047h)		0	1	0	0	0	1	1	1
R70h	Internal Use 28	*	*	GS	SS	TE MODE	TEON	CSEL[2:0]		
	initial (0006h)			0	0	0	0	1	1	0
	recommend (0066h)			1	1	0	0	1	1	0
R72h	Data control	*	*	*	DFM[1:0]		*	*	TRI[1:0]	
	initial (0000h)				0	0			0	0
	recommend (0000h)				0	0			0	0
R90h	Display Control 8	*	SAP[7:0]							
	initial (000Ah)		0	0	0	0	1	0	1	0
	recommend (007Fh)		0	1	1	1	1	1	1	1
R91h	Display Control 11	*	GEN_OFF[7:0]							
	initial (0014h)		0	0	0	1	0	1	0	0
	recommend (0014h)		0	0	0	1	0	1	0	0
R93h	OSC Control 3	*	*	*	*	*	RADJ[3:0]			
	initial (000Fh)						1	1	1	1
	recommend (000Fh)						1	1	1	1
R94h	SAP Idle mode	*	SAP_I[7:0]							
	initial (000Ah)		0	0	0	0	1	0	1	0
	recommend (000Ah)		0	0	0	0	1	0	1	0
R95h	DCCLK SYNC TO CL1	*	*	*	*	*	*	*	*	DCCLK_SYNC
	initial (0000h)									0
	recommend (0001h)									1
R96h	TEST1	*	*	*	*	*	*	*	*	TEST1
	initial (0000h)		0	0	0	0	0	0	0	0
	recommend (0000h)		0	0	0	0	0	0	0	0

## 10. Sequence

## 10.1 Power-ON Sequence

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
	RESETB=1											
	wait 1 msec or more											
	RESETB=0											
	wait 10 usec or more											
	RESETB=1											
	wait 120 msec or more											
TEST1 setting	TEST1	R96h	01h	*	0	0	0	0	0	0	0	1
OSC control setting	OSC Control 1	R19h	87h	*	CADJ[3:0]			CUADJ[2:0]			OSC_EN	
					1	0	0	0	0	1	1	1
	wait 10 msec or more											
Display OFF setting	Display Control 1	R26h	80h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	0	0	0	0	0	0
	Power Control 1	R1Bh	0Ch	*	GAS_ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	0	1	1	0	0
Power supply setting initializing	Power Control 6	R20h	00h	*	BT[3:0]			*	*	*	*	
					0	0	0	0	0	0	0	0
	Power Control 5	R1Fh	07h	*	*	*	*	*	VRH[3:0]			
					0	0	0	0	0	1	1	1
Power supply operation start setting	Power Control 2	R1Ch	04h	*	*	*	*	*	*	AP[2:0]		
					0	0	0	0	0	1	0	0
	Power Control 1	R1Bh	14h	*	GAS_ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	1	0	1	0	0
	wait 40 msec or more											
Power control setting	BGP Control	R42h	08h	*	*	*	*	VBGP_OE	BGP[3:0]			
					0	0	0	0	1	0	0	0
	Cycle Control 1	R23h	95h	*	N_DC[7:0]							
					1	0	0	1	0	1	0	1
Cycle Control 2	R24h	95h	*	PI_DC[7:0]								
					1	0	0	1	0	1	0	1
Cycle Control 3	R25h	FFh	*	I_DC[7:0]								
					1	1	1	1	1	1	1	1
Power Control 7	R21h	10h	*	*	*	FS1[1:0]		*	*	FS0[1:0]		
					0	0	0	1	0	0	0	0
Power Control 11	R2Bh	00h	*	*	*	PI_PRE_REFRESH[1:0]		BLANK_DIV[3:0]				
					0	0	0	0	0	0	0	0
DCCLK SYNC TO CL1	R95h	01h	*	*	*	*	*	*	*	*	*	DCCLK_SYNC
					0	0	0	0	0	0	0	1

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control setting	OSC Control 2	R1Ah	00h	*	*	*	*	*	*	*	*	OSC_TEST
				0	0	0	0	0	0	0	0	
	OSC Control 3	R93h	0Fh	*	*	*	*	*	RADJ[3:0]			
				0	0	0	0	1	1	1	1	
Internal Use 28	R70h	66h	*	*	GS	SS	TE	TEON	CSEL[2:0]			
			0	1	1	0	0	1	1	0		
Gate Scan control	R18h	01h	*	*	*	*	*	*	*	SCROL	SM	
			0	0	0	0	0	0	0	0	0	1
r control setting	r Control 1	R46h	86h	*	GSEL	CP1[2:0]			*	CP0[2:0]		
				1	0	0	0	0	1	1	0	
	r Control 2	R47h	60h	*	*	CN1[2:0]			*	CN0[2:0]		
				0	1	1	0	0	0	0	0	
	r Control 3	R48h	01h	*	*	NP1[2:0]			*	NP0[2:0]		
				0	0	0	0	0	0	0	1	
	r Control 4	R49h	67h	*	*	NP3[2:0]			*	NP2[2:0]		
				0	1	1	0	0	1	1	1	
	r Control 5	R4Ah	46h	*	*	NP5[2:0]			*	NP4[2:0]		
				0	1	0	0	0	1	1	0	
	r Control 6	R4Bh	13h	*	*	NN1[2:0]			*	NN0[2:0]		
				0	0	0	1	0	0	1	1	
	r Control 7	R4Ch	01h	*	*	NN3[2:0]			*	NN2[2:0]		
				0	0	0	0	0	0	0	1	
r Control 8	R4Dh	67h	*	*	NN5[2:0]			*	NN4[2:0]			
			0	1	1	0	0	1	1	1		
r Control 9	R4Eh	00h	*	CGMP1[1:0]	CGMP0[1:0]	OP0[3:0]						
			0	0	0	0	0	0	0	0		
r Control 10	R4Fh	13h	*	CGMP3	CGMP2	*	OP1[4:0]					
			0	0	0	1	0	0	1	1		
r Control 11	R50h	02h	*	CGMN1[1:0]	CGMN0[1:0]	ON0[3:0]						
			0	0	0	0	0	0	1	0		
r Control 12	R51h	00h	*	CGMN3	CGMN2	*	ON1[4:0]					
			0	0	0	0	0	0	0	0		
RGB interface control setting	RGB interface control 1	R38h	00h	*	*	*	*	RGB_EN	DPL	HSPL	VSPL	EPL
				0	0	0	0	0	0	0	0	
RGB interface control setting	RGB interface control 2	R39h	00h	*	DOTCLK_DIV[7:0]							
				0	0	0	0	0	0	0	0	
Display control setting	Display Control 2	R27h	02h	*	*	*	*	*	N_BP[3:0]			
				0	0	0	0	0	0	1	0	
	Display Control 3	R28h	03h	*	*	*	*	*	N_FP[3:0]			
				0	0	0	0	0	0	1	1	
	Display Control 4	R29h	08h	*	*	*	*	*	PI_BP[3:0]			
				0	0	0	0	1	0	0	0	
	Display Control 5	R2Ah	08h	*	*	*	*	*	PI_FP[3:0]			
				0	0	0	0	1	0	0	0	
	Display Control 6	R2Ch	08h	*	*	*	*	*	I_BP[3:0]			
				0	0	0	0	1	0	0	0	
	Display Control 7	R2Dh	08h	*	*	*	*	*	I_FP[3:0]			
				0	0	0	0	1	0	0	0	
Display Control 9	R35h	09h	*	EQS[7:0]								
			0	0	0	0	1	0	0	1		
Display Control 10	R36h	09h	*	EQP[7:0]								
			0	0	0	0	1	0	0	1		
Display Control 11	R91h	14h	*	GEN_OFF[7:0]								
			0	0	0	1	0	1	0	0		
Display Control 12	R37h	00h	*	*	*	PTG[1:0]	ISC[3:0]					
			0	0	0	0	0	0	0	0		

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Display control setting	Display Mode control	R01h	06h	*	*	*	*	*	IDMON	INVON	NORON	PTLON
				0	0	0	0	0	1	1	0	
	Cycle Control 1	R3Ah	A1h	*	N_RTN[3:0]			*	N_NW[2:0]			
				1	0	1	0	0	0	0	1	
	Cycle Control 2	R3Bh	A1h	*	PI_RTN[3:0]			*	PI_NW[2:0]			
				1	0	1	0	0	0	0	1	
	Cycle Control 3	R3Ch	A0h	*	I_RTN[3:0]			*	I_NW[2:0]			
				1	0	1	0	0	0	0	0	
Cycle Control 4	R3Dh	00h	*	*	*	DIV_I[1:0]		DIV_PI[1:0]		DIV_N[1:0]		
			0	0	0	0	0	0	0	0		
Cycle Control 5	R3Eh	2Dh	*	SON[7:0]								
			0	0	1	0	1	1	0	1		
Cycle Control 6	R40h	03h	*	GDON[7:0]								
			0	0	0	0	0	0	1	1		
Cycle Control 7	R41h	CCh	*	GDOF[7:0]								
			1	1	0	0	1	1	0	0		
Partial Image Display setting	Partial area start row 2	R0Ah	00h	*	PSL[15:8]							
				0	0	0	0	0	0	0	0	
	Partial area start row 1	R0Bh	00h	*	PSL[7:0]							
				0	0	0	0	0	0	0	0	
Partial area end row 2	R0Ch	01h	*	PEL[15:8]								
			0	0	0	0	0	0	0	1		
Partial area end row 1	R0Dh	3Fh	*	PEL[7:0]								
			0	0	1	1	1	1	1	1		
Vertical Scroll setting	Vertical Scroll Top fixed area 2	R0Eh	00h	*	TFA[15:8]							
				0	0	0	0	0	0	0	0	
	Vertical Scroll Top fixed area 1	R0Fh	00h	*	TFA[7:0]							
				0	0	0	0	0	0	0	0	
	Vertical Scroll height area 2	R10h	01h	*	VSA[15:8]							
				0	0	0	0	0	0	0	1	
	Vertical Scroll height area 1	R11h	40h	*	VSA[7:0]							
				0	1	0	0	0	0	0	0	
Vertical Scroll Button area 2	R12h	00h	*	BFA[15:8]								
			0	0	0	0	0	0	0	0		
Vertical Scroll Button area 1	R13h	00h	*	BFA[7:0]								
			0	0	0	0	0	0	0	0		
Vertical Scroll Start address 2	R14h	00h	*	VSP[15:8]								
			0	0	0	0	0	0	0	0		
Vertical Scroll Start address 1	R15h	00h	*	VSP[7:0]								
			0	0	0	0	0	0	0	0		
Window address setting	Column address start 2	R02h	00h	*	SC[15:8]							
				0	0	0	0	0	0	0	0	
	Column address start 1	R03h	00h	*	SC[7:0]							
				0	0	0	0	0	0	0	0	
	Column address end 2	R04h	00h	*	EC[15:8]							
				0	0	0	0	0	0	0	0	
	Column address end 1	R05h	EFh	*	EC[7:0]							
				1	1	1	0	1	1	1	1	
	Row address start 2	R06h	00h	*	SP[15:8]							
				0	0	0	0	0	0	0	0	
Row address start 1	R07h	00h	*	SP[7:0]								
			0	0	0	0	0	0	0	0		
Row address end 2	R08h	01h	*	EP[15:8]								
			0	0	0	0	0	0	0	1		
Row address end 1	R09h	3Fh	*	EP[7:0]								
			0	0	1	1	1	1	1	1		
Memory Access control	R16h	08h	*	MY	MX	MV	*	BGR	*	*	*	
			0	0	0	0	1	0	0	0		
Data control	R72h	00h	*	*	*	DFM[1:0]		*	*	TRI[1:0]		
			0	0	0	0	0	0	0	0	0	

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Window address setting	Write Data	R22h		GRAM Write Data								
	wait 60 msec or more											
Display on setting	SAP Idle mode	R94h	0Ah	*	SAP_I[7:0]							
					0	0	0	0	1	0	1	0
	Display Control 8	R90h	7Fh	*	SAP[7:0]							
					0	1	1	1	1	1	1	1
	Display Control 1	R26h	84h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	0	0	0	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	A4h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
				1	0	1	0	0	1	0	0	
Display Control 1	R26h	ACh	*	PT[1:0]		GON	DTE	D[1:0]		*	*	
				1	0	1	0	1	1	0	0	
wait 40 msec or more												
Display Control 1	R26h	BCh	*	PT[1:0]		GON	DTE	D[1:0]		*	*	
				1	0	1	1	1	1	0	0	
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0

## 10.2 Power-OFF Sequence ( Stand-by Transit Sequence )

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
TEST1 setting	TEST1	R96h	01h	*	0	0	0	0	0	0	0	1	
	Display Control 1	R26h	B8h	*	PT[1:0]		GON	DTE	D[1:0]		*	*	
					1	0	1	1	1	0	0	0	
	wait 40 msec or more												
	Display Control 1	R26h	A8h	*	PT[1:0]		GON	DTE	D[1:0]		*	*	
					1	0	1	0	1	0	0	0	
	Display Control 1	R26h	84h	*	PT[1:0]		GON	DTE	D[1:0]		*	*	
				1	0	0	0	0	1	0	0		
wait 40 msec or more													
Display Control 1	R26h	80h	*	PT[1:0]		GON	DTE	D[1:0]		*	*		
				1	0	0	0	0	0	0	0		
Power off setting	Display Control 8	R90h	00h	*	SAP[7:0]								
					0	0	0	0	0	0	0	0	
	Power Control 2	R1Ch	00h	*	*	*	*	*	*	AP[2:0]			
					0	0	0	0	0	0	0	0	
	Power Control 1	R1Bh	04h	*	GAS ENB		*	*	PON	DK	XDK	VLCD_TRI	STB
				0	0	0	0	0	0	1	0	0	
VCOM Control 1	R43h	00h	*	VCOM G		*	*	*	*	*	*	*	
				0	0	0	0	0	0	0	0	0	
Power Control 1	R1Bh	0Ch	*	GAS ENB		*	*	PON	DK	XDK	VLCD_TRI	STB	
				0	0	0	0	0	1	1	0	0	
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0	
Power off setting	Power Control 1	R1Bh	0Dh	*	GAS ENB		*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	0	1	1	0	1	
OSC control setting	OSC Control 1	R19h	86h	*	CADJ[3:0]				CUADJ[2:0]			OSC_EN	
					1	0	0	0	0	1	1	0	

## 10.3 Stand-by Release Sequence

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control setting	OSC Control 1	R19h	87h	*	CADJ[3:0]				CUADJ[2:0]			OSC_EN
					1	0	0	0	0	1	1	
	wait 10 msec or more											
	Power Control 1	R1Bh	0Ch	*	GAS ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	0	1	1	0	0
Power supply setting initializing	Power Control 6	R20h	00h	*	BT[3:0]				*	*	*	*
					0	0	0	0	0	0	0	0
	Power Control 5	R1Fh	07h	*	*	*	*	*	VRH[3:0]			
					0	0	0	0	0	1	1	1
	VCOM Control 2	R44h	7Fh	*	*	VCM[6:0]						
					0	1	1	1	1	1	1	1
	VCOM Control 3	R45h	14h	*	*	*	*	VDV[4:0]				
				0	0	0	1	0	1	0	0	
	Power Control 3	R1Dh	05h	*	*	*	*	*	*	VC1[2:0]		
				0	0	0	0	0	0	1	0	1
	Power Control 4	R1Eh	00h	*	*	*	*	*	*	VC3[2:0]		
				0	0	0	0	0	0	0	0	0
Power supply operation start setting	Power Control 2	R1Ch	04h	*	*	*	*	*	*	AP[2:0]		
					0	0	0	0	0	1	0	0
	Power Control 1	R1Bh	14h	*	GAS ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	1	0	1	0	0
	wait 40 msec or more											
	VCOM Control 1	R43h	80h	*	VCOM G	*	*	*	*	*	*	
					1	0	0	0	0	0	0	0
	wait 60 msec or more											
Display on setting	Display Control 8	R90h	7Fh	*	SAP[7:0]							
					0	1	1	1	1	1	1	1
TEST1 setting	TEST1	R96h	01h	*	0	0	0	0	0	0	0	1
Display on setting	Display Control 1	R26h	84h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	0	0	0	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	A4h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	0	0	1	0	0
	Display Control 1	R26h	ACH	*	PT[1:0]		GON	DTE	D[1:0]		*	*
				1	0	1	0	1	1	0	0	
	wait 40 msec or more											
	Display Control 1	R26h	BCh	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	1	1	1	0	0
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0



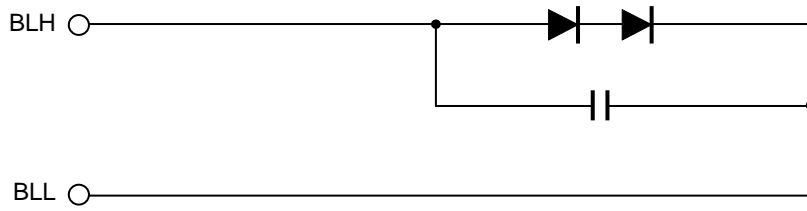
## 10.4 Refresh Sequence

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control setting	OSC Control 1	R19h	87h	*	CADJ[3:0]			CUADJ[2:0]			OSC_EN	
				1	0	0	0	0	1	1	1	
Power supply setting initializing	Power Control 6	R20h	00h	*	BT[3:0]			*	*	*	*	
					0	0	0	0	0	0	0	
	Power Control 5	R1Fh	07h	*	*	*	*	*	VRH[3:0]			
					0	0	0	0	0	1	1	1
	VCOM Control 2	R44h	7Fh	*	*	VCM[6:0]						
					0	1	1	1	1	1	1	1
	VCOM Control 3	R45h	14h	*	*	*	*	VDV[4:0]				
				0	0	0	1	0	1	0	0	
	Power Control 3	R1Dh	05h	*	*	*	*	*	VC1[2:0]			
					0	0	0	0	0	1	0	1
	Power Control 4	R1Eh	00h	*	*	*	*	*	VC3[2:0]			
					0	0	0	0	0	0	0	0
Power supply operation start setting	Power Control 2	R1Ch	04h	*	*	*	*	*	AP[2:0]			
					0	0	0	0	0	1	0	0
	Power Control 1	R1Bh	14h	*	GAS ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	1	0	1	0	0
	VCOM Control 1	R43h	80h	*	VCOM G	*	*	*	*	*	*	*
					1	0	0	0	0	0	0	0
Power control setting	BGP Control	R42h	08h	*	*	*	*	VBGP_OE	BGP[3:0]			
					0	0	0	0	1	0	0	0
	Cycle Control 1	R23h	95h	*	N_DC[7:0]							
					1	0	0	1	0	1	0	1
	Cycle Control 2	R24h	95h	*	PI_DC[7:0]							
					1	0	0	1	0	1	0	1
	Cycle Control 3	R25h	FFh	*	I_DC[7:0]							
					1	1	1	1	1	1	1	1
	Power Control 7	R21h	10h	*	*	*	FS1[1:0]		*	*	FS0[1:0]	
					0	0	0	1	0	0	0	0
	Power Control 11	R2Bh	00h	*	*	*	PI_PRE_REFRESH[1:0]		BLANK_DIV[3:0]			
					0	0	0	0	0	0	0	0
	DCCLK SYNC TO CL1	R95h	01h	*	*	*	*	*	*	*	*	DCCLK_SYNC
					0	0	0	0	0	0	0	1
OSC control setting	OSC Control 2	R1Ah	00h	*	*	*	*	*	*	*	*	OSC_TEST
					0	0	0	0	0	0	0	0
	OSC Control 3	R93h	0Fh	*	*	*	*	*	RADJ[3:0]			
					0	0	0	0	1	1	1	1
	Internal Use 28	R70h	66h	*	*	GS	SS	TE MODE	TEON	CSEL[2:0]		
					0	1	1	0	0	1	1	0
	Gate Scan control	R18h	01h	*	*	*	*	*	*	*	SCROL_ON	SM
					0	0	0	0	0	0	0	1

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
r control setting	r Control 1	R46h	86h	*	GSEL	CP1[2:0]			*	CP0[2:0]		
					1	0	0	0	0	1	1	0
	r Control 2	R47h	60h	*	*	CN1[2:0]			*	CN0[2:0]		
					0	1	1	0	0	0	0	0
	r Control 3	R48h	01h	*	*	NP1[2:0]			*	NP0[2:0]		
					0	0	0	0	0	0	0	1
	r Control 4	R49h	67h	*	*	NP3[2:0]			*	NP2[2:0]		
					0	1	1	0	0	1	1	1
	r Control 5	R4Ah	46h	*	*	NP5[2:0]			*	NP4[2:0]		
					0	1	0	0	0	1	1	0
	r Control 6	R4Bh	13h	*	*	NN1[2:0]			*	NN0[2:0]		
					0	0	0	1	0	0	1	1
r Control 7	R4Ch	01h	*	*	NN3[2:0]			*	NN2[2:0]			
				0	0	0	0	0	0	0	1	
r Control 8	R4Dh	67h	*	*	NN5[2:0]			*	NN4[2:0]			
				0	1	1	0	0	1	1	1	
r Control 9	R4Eh	00h	*	CGMP1[1:0]	CGMP0[1:0]	OP0[3:0]						
				0	0	0	0	0	0	0	0	0
r Control 10	R4Fh	13h	*	CGMP3	CGMP2	*	OP1[4:0]					
				0	0	0	1	0	0	1	1	
r Control 11	R50h	02h	*	CGMN1[1:0]	CGMN0[1:0]	ON0[3:0]						
				0	0	0	0	0	0	1	0	
r Control 12	R51h	00h	*	CGMN3	CGMN2	*	ON1[4:0]					
				0	0	0	0	0	0	0	0	
RGB interface control setting	RGB interface control 1	R38h	00h	*	*	*	*	RGB_EN	DPL	HSPL	VSPL	EPL
					0	0	0	0	0	0	0	0
RGB interface control setting	RGB interface control 2	R39h	00h	*	DOTCLK_DIV[7:0]							
					0	0	0	0	0	0	0	0
Display control setting	Display Control 2	R27h	02h	*	*	*	*	*	N_BP[3:0]			
					0	0	0	0	0	0	1	0
	Display Control 3	R28h	03h	*	*	*	*	*	N_FP[3:0]			
					0	0	0	0	0	0	1	1
	Display Control 4	R29h	08h	*	*	*	*	*	PI_BP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 5	R2Ah	08h	*	*	*	*	*	PI_FP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 6	R2Ch	08h	*	*	*	*	*	I_BP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 7	R2Dh	08h	*	*	*	*	*	I_FP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 9	R35h	09h	*	EQS[7:0]							
					0	0	0	0	1	0	0	1
	Display Control 10	R36h	09h	*	EQP[7:0]							
					0	0	0	0	1	0	0	1
Display Control 11	R91h	14h	*	GEN_OFF[7:0]								
				0	0	0	1	0	1	0	0	
Display Control 12	R37h	00h	*	*	*	PTG[1:0]	ISC[3:0]					
				0	0	0	0	0	0	0	0	
Display Mode control	R01h	06h	*	*	*	*	*	IDMON	INVON	NORON	PTLON	
				0	0	0	0	0	1	1	0	
Cycle Control 1	R3Ah	A1h	*	N_RTN[3:0]				*	N_NW[2:0]			
				1	0	1	0	0	0	0	1	
Cycle Control 2	R3Bh	A1h	*	PI_RTN[3:0]				*	PI_NW[2:0]			
				1	0	1	0	0	0	0	1	
Cycle Control 3	R3Ch	A0h	*	I_RTN[3:0]				*	I_NW[2:0]			
				1	0	1	0	0	0	0	0	
Cycle Control 4	R3Dh	00h	*	*	*	DIV_I[1:0]	DIV_PI[1:0]	DIV_N[1:0]				
				0	0	0	0	0	0	0	0	

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Display control setting	Cycle Control 5	R3Eh	2Dh	*	SON[7:0]							
					0	0	1	0	1	1	0	1
	Cycle Control 6	R40h	03h	*	GDON[7:0]							
					0	0	0	0	0	0	1	1
	Cycle Control 7	R41h	CCh	*	GDOF[7:0]							
					1	1	0	0	1	1	0	0
Patial Image Display setting	Partial area start row 2	R0Ah	00h	*	PSL[15:8]							
					0	0	0	0	0	0	0	0
	Partial area start row 1	R0Bh	00h	*	PSL[7:0]							
					0	0	0	0	0	0	0	0
	Partial area end row 2	R0Ch	01h	*	PEL[15:8]							
					0	0	0	0	0	0	0	1
	Partial area end row 1	R0Dh	3Fh	*	PEL[7:0]							
					0	0	1	1	1	1	1	1
Vertical Scroll setting	Vertical Scroll Top fixed area 2	R0Eh	00h	*	TFA[15:8]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Top fixed area 1	R0Fh	00h	*	TFA[7:0]							
					0	0	0	0	0	0	0	0
	Vertical Scroll height area 2	R10h	01h	*	VSA[15:8]							
					0	0	0	0	0	0	0	1
	Vertical Scroll height area 1	R11h	40h	*	VSA[7:0]							
					0	1	0	0	0	0	0	0
	Vertical Scroll Button area 2	R12h	00h	*	BFA[15:8]							
				0	0	0	0	0	0	0	0	
Vertical Scroll Button area 1	R13h	00h	*	BFA[7:0]								
				0	0	0	0	0	0	0	0	
	Vertical Scroll Start address 2	R14h	00h	*	VSP[15:8]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Start address 1	R15h	00h	*	VSP[7:0]							
					0	0	0	0	0	0	0	0
Window address setting	Column address start 2	R02h	00h	*	SC[15:8]							
					0	0	0	0	0	0	0	0
	Column address start 1	R03h	00h	*	SC[7:0]							
					0	0	0	0	0	0	0	0
	Column address end 2	R04h	00h	*	EC[15:8]							
					0	0	0	0	0	0	0	0
	Column address end 1	R05h	EFh	*	EC[7:0]							
					1	1	1	0	1	1	1	1
	Row address start 2	R06h	00h	*	SP[15:8]							
					0	0	0	0	0	0	0	0
Row address start 1	R07h	00h	*	SP[7:0]								
				0	0	0	0	0	0	0	0	
	Row address end 2	R08h	01h	*	EP[15:8]							
					0	0	0	0	0	0	0	1
	Row address end 1	R09h	3Fh	*	EP[7:0]							
					0	0	1	1	1	1	1	1
	Memory Access control	R16h	08h	*	MY	MX	MV	*	BGR	*	*	*
					0	0	0	0	1	0	0	0
	Data control	R72h	00h	*	*	*	DFM[1:0]	*	*	*	TRI[1:0]	
					0	0	0	0	0	0	0	0
Display on setting	SAP Idle mode	R94h	0Ah	*	SAP_I[7:0]							
					0	0	0	0	1	0	1	0
	Display Control 8	R90h	7Fh	*	SAP[7:0]							
					0	1	1	1	1	1	1	1
	Display Control 1	R26h	BCh	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	1	1	1	0	0
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0

11. LED Circuit



## 12. Characteristics

## 12.1 Optical Characteristics

&lt; Measurement Condition &gt;

Measuring instruments: CS1000 (KONICA MINOLTA) , LCD7200(OTSUKA ELECTRONICS) ,  
EZcontrast160D (ELDIM)

Driving condition: VCI = IOVCC = 2.7V, VSS = 0V  
Optimized VCOMDC

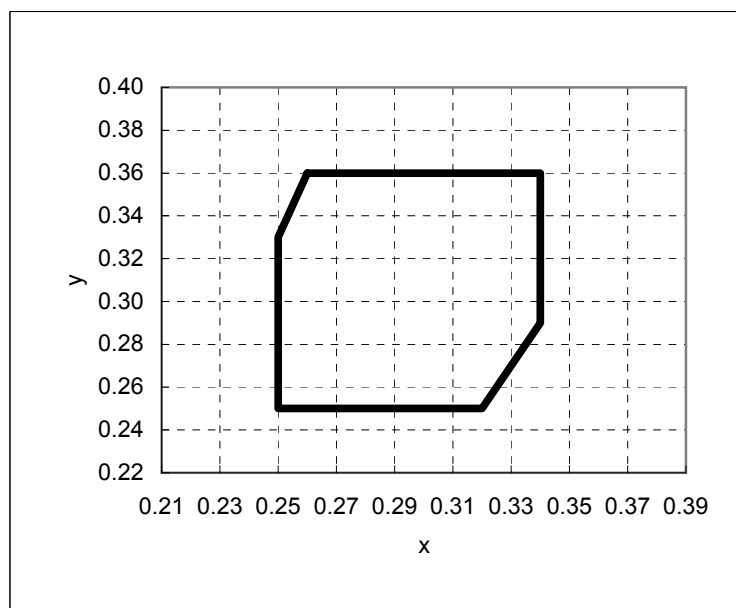
Backlight: IL=7.5mA

Measured temperature: Ta=25° C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Remark
Response time	Rise time	TON	[Data]= 3Fh→00h	—	—	40	ms	1	※
	Fall time	TOFF	[Data]= 00h→3Fh	—	—	60	ms		
Contrast ratio	Backlight ON	CR	[Data]= 3Fh/00h	240	400	—		2	
	Backlight OFF			—	8.5	—			
Viewing angle	Left	θL	[Data]= 3Fh/00h CR ≥ 10	80	—	—	deg	3	※
	Right	θR		80	—	—	deg		
	Up	φU		80	—	—	deg		
	Down	φD		80	—	—	deg		
White Chromaticity	x	[Data]=3Fh	White chromaticity range					4	
	y								
Burn-in				No noticeable burn-in image shall be observed after 2 hours of window pattern display.				5	
Center brightness			[Data]=3Fh	210	300	—	cd/m <sup>2</sup>	6	
Brightness distribution			[Data]=3Fh	70	—	—	%	7	

\* Note number 1 to 7: Refer to the APPENDIX of "Reference Method for Measuring Optical Characteristics".

※ Measured in the form of LCD module.



White Chromaticity Range

【White Chromaticity Range】

x	y
0.26	0.36
0.25	0.33
0.25	0.25
0.32	0.25
0.34	0.29
0.34	0.36

## 12.2 Temperature Characteristics

< Measurement Condition >

Measuring instruments: CS1000 (KONICA MINOLTA) , LCD7200(OTSUKA ELECTRONICS)

Driving condition: VCI = IOVCC = 2.7V, VSS = 0V

Optimized VCOMDC

Backlight: IL=7.5mA

Item		Specification		Remark	
		Ta = -20° C	Ta = 70° C		
Contrast ratio	CR	40 or more	40 or more	Backlight ON	
Response time	Rise time	TON	200 msec or less	30 msec or less	※
	Fall time	TOFF	300 msec or less	50 msec or less	※
Display Quality		No noticeable display defect or nonuniformity should be observed.		Use the criteria for judgment specified in the section 13.	

※ Measured in the form of LCD module.

13. Criteria of Judgment

13.1 Defective Display and Screen Quality

Test Condition: Observed TFT-LCD monitor from front during operation with the following conditions  
 Driving Signal Raster Patter (RGB, white, black)  
 Signal condition [Data]:3Fh,2Ah,00h(3steps)  
 Observation distance 30 cm  
 Illuminance 200 to 350 lx  
 Backlight IL=7.5mA

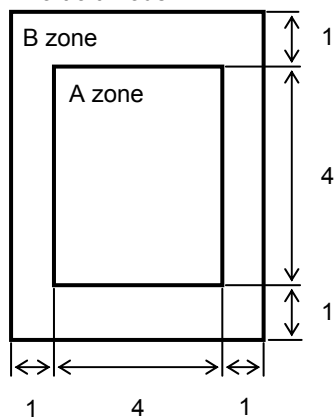
Defect item		Defect content	Criteria	
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots	Not exists	
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot)	Refer to table 1	
		High bright dot: Visible through 2% ND filter at [Data]=00h		
		Low bright dot: Visible through 5% ND filter at [Data]=00h Dark dot: Appear dark through white display at [Data]=2Ah Invisible through 5% ND filter at [Data]=00h		ignored
Screen Quality	Dirt	Uneven brightness (white stain, black stain etc)	Invisible through 1% ND filter	
	Foreign particle	Point-like	$0.25\text{mm} < \phi$	$N=0$
			$0.20\text{mm} < \phi \leq 0.25\text{mm}$	$N \leq 2$
			$\phi \leq 0.20\text{mm}$	Ignored
		Liner	$3.0\text{mm} < \text{length and } 0.08\text{mm} < \text{width}$	$N=0$
	$\text{length} \leq 3.0\text{mm or width} \leq 0.08\text{mm}$		Ignored	
Others		Use boundary sample for judgment when necessary		

$\phi(\text{mm})$ : Average diameter = (major axis + minor axis)/2  
 Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
B	2	4	4	5	
Total	2	4	4	5	

<Portrait model>



Division of A and B areas

B area: Active area

Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

## 13.2 Screen and Other Appearance

## Testing conditions

Observation distance	30cm
Illuminance	1200~2000 lx

Item		Criteria	Remark
Polarizer	Flaw	Ignore invisible defect when the backlight is on.	Applicable area: Active area only (Refer to the section 3.2 "Outward form")
	Stain		
	Bubble		
	Dust		
	Dent		
S-case		No functional defect occurs	
FPC cable		No functional defect occurs	



## 14. Reliability Test

Test item		Test condition		number of failures /number of examinations
Durability test	High temperature storage	Ta=80° C	240hr	0/3
	Low temperature storage	Ta=-30° C	240hr	0/3
	High temperature & high humidity storage	Ta=60° C, RH=90% non condensing	240hr	0/3
	High temperature operation	Tp=70° C	240hr	0/3
	Low temperature operation	Tp=-20° C	240hr	0/3
	High temp & humid operation	Tp=40° C, RH=90% non condensing	240hr	0/3
	Thermal shock storage	-30←→80° C(30min/30min)	100 cycles	0/3
Mechanical environmental test	Electrostatic discharge test (Non operation)	Confirms to EIAJ ED-4701/300 C=200pF,R=0Ω,V=±200V Each 3 times of discharge on and power supply and other terminals.		0/3
	Surface discharge test (Non operation)	C=250pF, R=100Ω, V=±12kV Each 5 times of discharge in both polarities on the center of screen with the case grounded.		0/3
	Vibration test	Total amplitude 1.5mm, f=10~55Hz, X,Y,Z directions for each 2 hours		0/3
	Impact test	Use ORTUS TECHNOLOGY original jig (see next page)and make an impact with peak acceleration of 1000m/s <sup>2</sup> for 6 msec with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-2011.		0/3
Packing test	Packing vibration-proof test	Acceleration of 19.6m/s <sup>2</sup> with frequency of 10→55→10Hz, X,Y, Zdirection for each 30 minutes		0/1 Packing
	Packing drop test	Drop from 75cm high. 1 time to each 6 surfaces, 3 edges, 1 corner		0/1 Packing

Note: Ta=ambient temperature Tp=Panel temperature

※ The profile of high temperature/humidity storage and High Temperature/humidity operation (Pure water of over 10MΩ·cm shall be used.)

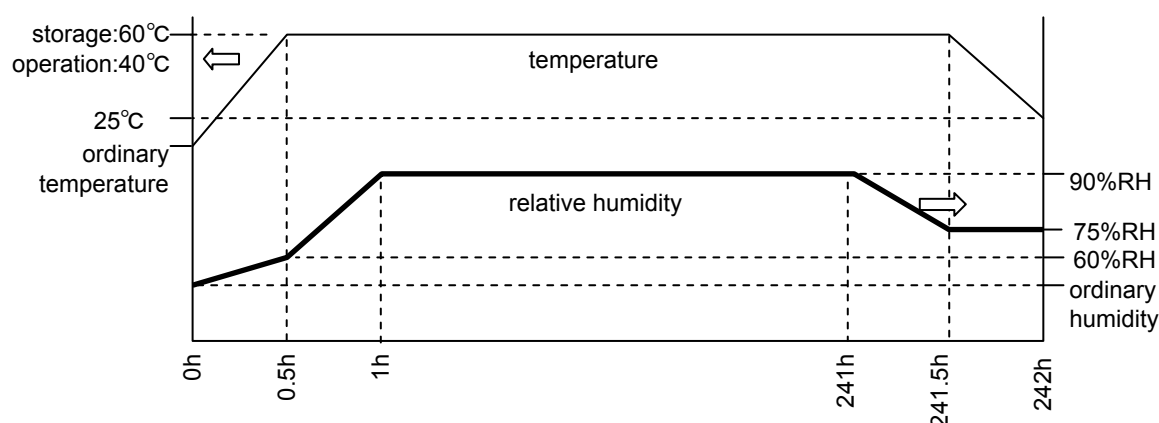
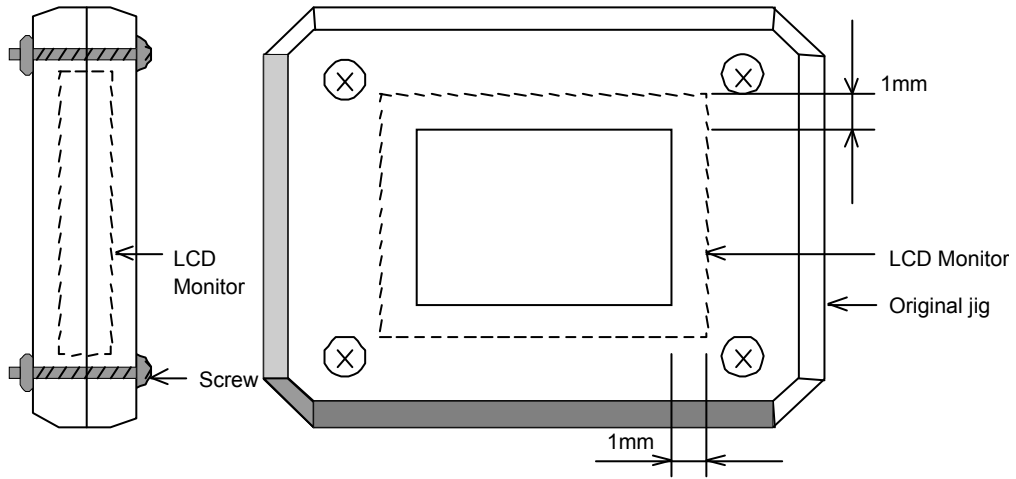


Table2.Reliability Criteria

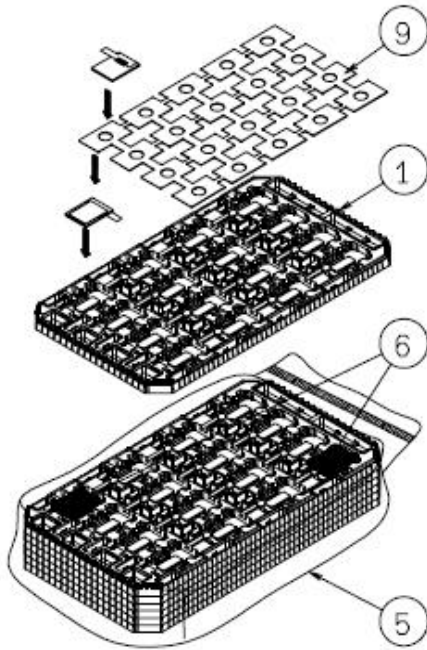
Measure the parameters after leaving the monitor at the ordinary temperature for 24 hours or more after the test completion.

item	Standard	Remarks
Display quality	No visible abnormality shall be seen.	As criteria of "13 Criteria of Judgment".
Contrast ratio	40 or more	Backlight ON

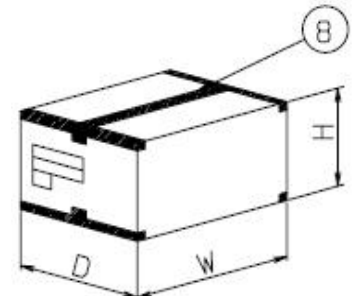
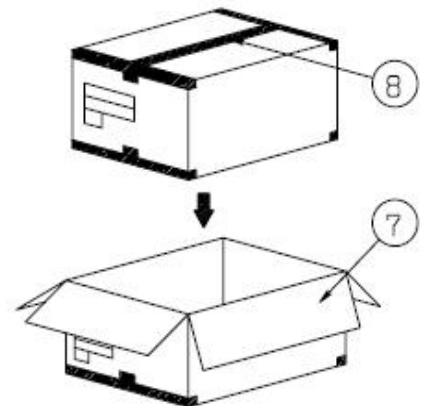
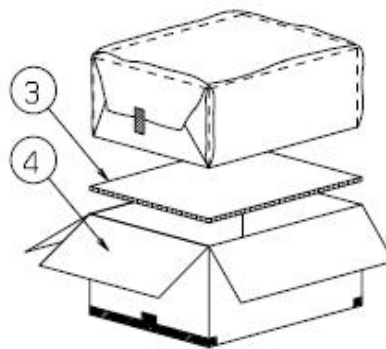
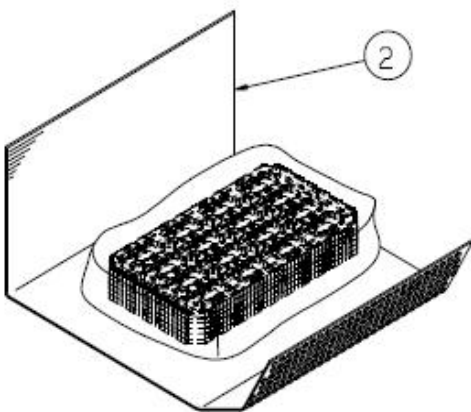
ORTUS TECHNOLOGY Original Jig



## 15. Packing Specifications



- Step1. • Each lower products are to be placed in one of the cut-outs of the tray with the LCD surface facing upward, and foam-sheet is put on products.  
• Upper products are to be placed with the LCD surface facing downward.
- Step2. • Trays be in a stack of 5.  
• One empty tray is to be put on the top of stack of 5 packed trays.
- Step3. • 2 packs of moisture absorbers are to be placed on the top tray as shown in the drawing.  
• Put piled trays into a sealing bag.
- Step4. • Vacuum and seal the sealing bag with the vacuum sealing machine.
- Step5. • The piled trays are to be wrapped with a bubble cushioning sheet., and to be fixed with adhesive tape.
- Step6. • A corrugated board is to be placed in the bottom of an outer carton.  
• The wrapped trays are to be put on the corrugated board in the outer carton.
- Step7. • The outer carton is to be sealed in H-shape with packing tape as shown in the drawing.  
• The model number, quantity of products, and shipping date are to be printed on the 2 opposite sides of the outer carton with black ink.  
• In necessary, shipping labels or impression markings are to be put on the outer carton.
- Step8. • The outer carton is to be inserted into a extra outer carton with same orientation.  
• The extra outer carton is to be sealed H-shape with packing tape as shown in the drawing.
- Step9. • The model number, quantity of products, and shipping date are to be printed on the 2 opposite sides of the extra outer carton with black ink.  
• In necessary, shipping labels or impression markings are to be put on the extra outer carton.



	Packing item name	Spec.,Material
①	TRAY	A-PET
②	B SHEET A	Anti-static air babble sheet
③	INNER BOARD	Corrugated cardboard
④	OUTER CARTON	Corrugated cardboard
⑤	SEALING BAG	
⑥	Drier	Moisture absorber
⑦	EXTRA OUTER CARTON	Corrugated cardboard
⑧	Packing tape	
⑧	FOAM SHEET	Anti-static polyethylene

Dimension of extra outer carton	
D : Approx.	(337mm)
W: Approx.	(618mm)
H: Approx.	(179mm)
Quantity of products packed in one carton:	200
Gross weight : Approx.	5.4Kg

## 16. Handling Instruction

## 16.1 Cautions for Handling LCD panels

**Caution**

- (1) Do not make an impact on the LCD panel glass because it may break and you may get injured from it.
- (2) If the glass breaks, do not touch it with bare hands.  
(Fragment of broken glass may stick you or you cut yourself on it.)
- (3) If you get injured, receive adequate first aid and consult a medial doctor.
- (4) Do not let liquid crystal get into your mouth.  
(If the LCD panel glass breaks, try not let liquid crystal get into your mouth even toxic property of liquid crystal has not been confirmed.)
- (5) If liquid crystal adheres, rinse it out thoroughly.  
(If liquid crystal adheres to your cloth or skin, wipe it off with rubbing alcohol or wash it thoroughly with soap. If liquid crystal gets into eyes, rinse it with clean water for at least 15 minutes and consult an eye doctor.)
- (6) If you scrap this products, follow a disposal standard of industrial waste that is legally valid in the community, country or territory where you reside.
- (7) Do not connect or disconnect this product while its application products is powered on.
- (8) Do not attempt to disassemble or modify this product as it is precision component.
- (9) If a part of soldering part has been exposed, and avoid contact (short-circuit) with a metallic part of the case etc. about FPC of this model, please.  
Please insulate it with the insulating tape etc. if necessary.  
The defective operation is caused, and there is a possibility to generation of heat and the ignition.
- (10) Since excess current protection circuit is not built in this TFT module, there is the possibility that LCD module or peripheral circuit become feverish and burned in case abnormal operation is generated.  
We recommend you to add excess current protection circuit to power supply.

**Caution**

**This mark is used to indicate a precaution or an instruction which, if not correctly observed, may result in bodily injury, or material damages alone.**

## 16.2 Precautions for Handling

- 1) Wear finger tips at incoming inspection and for handling the TFT monitors to keep display quality and keep the working area clean.  
Do not touch the surface of the monitor as it is easily scratched.
- 2) Wear grounded wrist-straps and use electrostatic neutralization blowers to prevent static charge and discharge when handling the TFT monitors as the LED in this TFT monitors is damageable to electrostatic discharge.  
Designate an appropriate operating area, and set equipment, tools, and machines properly when handling this product.
- 3) Avoid strong mechanical shock including knocking, hitting or dropping to the TFT monitors for protecting their glass parts. Do not use the TFT monitors that have been experienced dropping or strong mechanical shock.
- 4) Do not use or storage the TFT monitors at high temperature and high humidity environment. Particularly, never use or storage the TFT monitors at a location where condensation builds up.
- 5) Avoid using and storing TFT monitors at a location where they are exposed to direct sunlight or ultraviolet rays to prevent the LCD panels from deterioration by ultraviolet rays.
- 6) Do not stain or damage the contacts of the FPC cable .  
FPC cable needs to be inserted until it can reach to the end of connector slot.  
During insertion, make sure to keep the cable in a horizontal position to avoid an oblique insertion.  
Otherwise, it may cause poor contact or deteriorate reliability of the FPC cable.
- 7) The FPC cable is a design very weak to the bend and the pull as it is fixed with the tape.  
Do not bend or pull the FPC cable or carry the TFT monitor by holding the FPC cable.
- 8) Peel off the protective film on the TFT monitors during mounting process.  
Refer to the section 16.5 on how to peel off the protective film.  
We are not responsible for electrostatic discharge failures or other defects occur when peeling off the protective film.

## 16.3 Precautions for Operation

- 1) Since this TFT monitors are not equipped with light shielding for the driver IC, do not expose the driver IC to strong lights during operation as it may cause functional failures.
- 2) In case of powering up or powering off this LCD module, be sure to comply the sequence as instructed in this specification.
- 3) Do not plug in or out the FPC cable while power supply is switch on.  
Plug the FPC cable in and out while power supply is switched off.
- 4) Do not operate the TFT monitors in the strong magnetic field. It may break the TFT monitors.
- 5) Do not display a fixed image on the screen for a long time.  
Use a screen-saver or other measures to avoid a fixed image displayed on the screen for a long time. Otherwise, it may cause burn-in image on the screen due the characteristics of liquid crystal.

## 16.4 Storage Condition for Shipping Cartons

### Storage environment

- Temperature 0 to 40° C
- Humidity 60%RH or less  
No-condensing occurs under low temperature with high humidity condition.
- Atmosphere No poisonous gas that can erode electronic components and/or wiring materials should be detected.
- Time period 1 year
- Unpacking To prevent damages caused by static electricity, anti-static precautionary measures (e.g. earthing, anti-static mat) should be implemented.
- Maximum piling up 7 cartons

## 16.5 Precautions for Peeling off the Protective film

The followings work environment and work method are recommended to prevent the TFT monitors from static damage or adhesion of dust when peeling off the protective films.

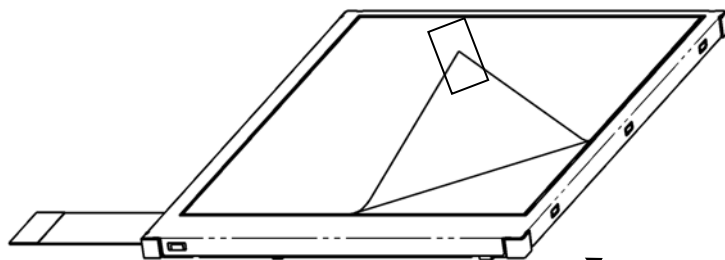
### A) Work Environment

- a) Humidity: 50 to 70 %RH, Temperature 15 to 27° C
- b) Operators should wear conductive shoes, conductive clothes, conductive finger tips and grounded wrist-straps. Anti-static treatment should be implemented to work area's floor.
- c) Use a room shielded against outside dust with sticky floor mat laid at the entrance to eliminate dirt.

### B) Work Method

The following procedures should taken to prevent the driver ICs from charging and discharging.

- a) Use an electrostatic neutralization blower to blow air on the TFT monitors to its lower right when the LCD-FPC cable is facing to the leftside.  
Optimize direction of the blowing air and the distance between the TFT monitors and the electrostatic neutralization blower.
- b) Put an adhesive tape (Scotch tape, etc) at the lower right corner area of the protective film to prevent scratch on surface of TFT monitors.
- c) Peel off the adhesive tape slowly (spending more than 2 secs to complete) by pulling it to opposite direction.



Direction of blowing air  
(Optimize air direction and the distance)

**APPENDIX**

Reference Method for Measuring Optical Characteristics and Performance

1. Measurement Condition (Backlight ON)

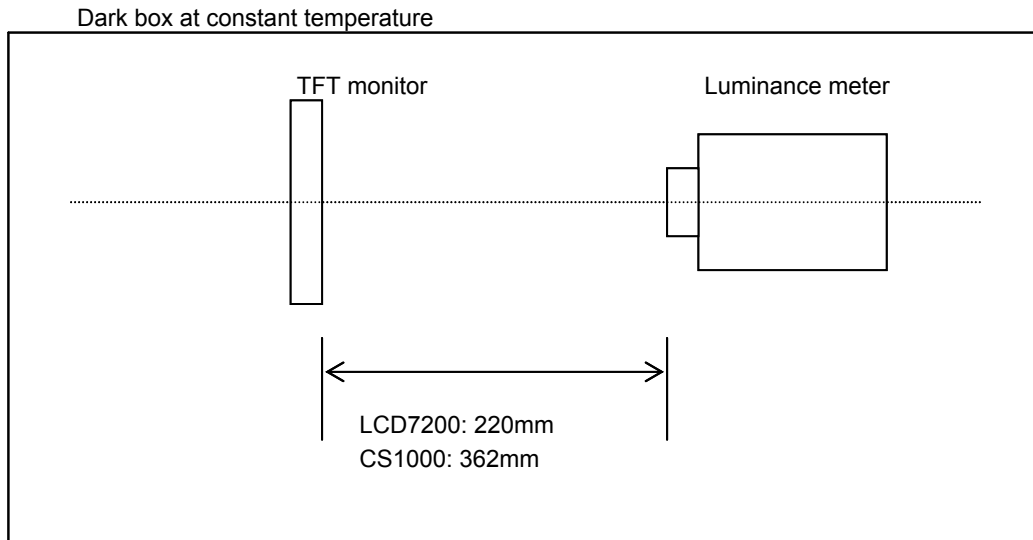
Measuring instruments: CS1000 (KONICA MINOLTA) , LCD7200(OTSUKA ELECTRONICS) ,EZcontrast160D (ELDIM)

Driving condition: Refer to the section "Optical Characteristics"

Measured temperature: 25° C unless specified

Measurement system: See the chart below. The luminance meter is placed on the normal line of measurement system.

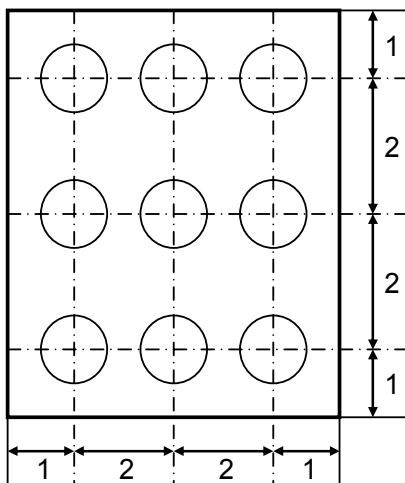
Measurement point: At the center of the screen unless otherwise specified



Measurement is made after 30 minutes of lighting of the backlight.

Measurement point: At the center point of the screen  
Brightness distribution: 9 points shown in the following drawing.

<Portrait model>

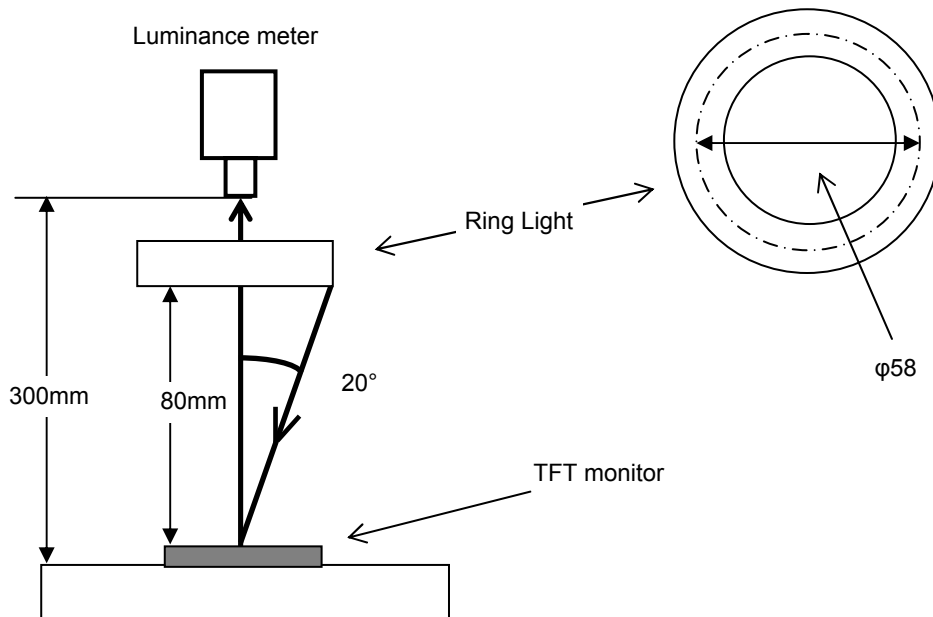


Dimensional ratio of active area

Backlight IL=7.5mA

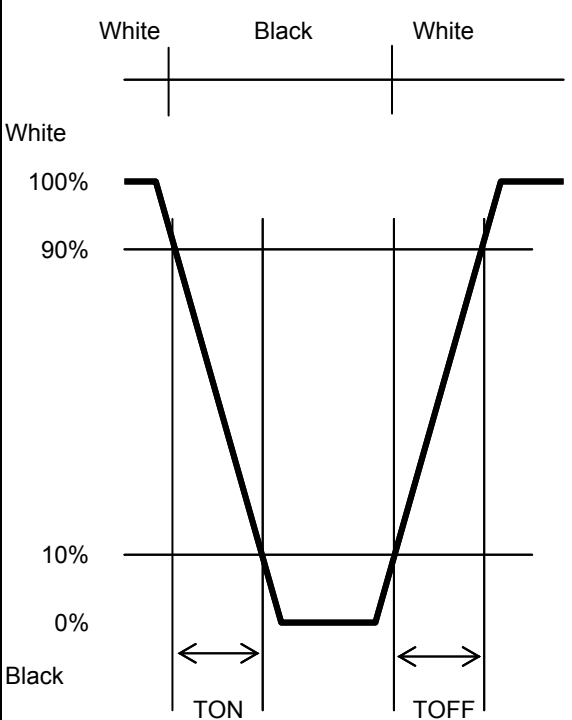
Measurement Condition (Contrast ratio Backlight OFF only)

- Measuring instruments: LCD7200(OTSUKA ELECTRONICS),Ring Light(40,000 lx, $\phi$ 58)
- Driving condition: Refer to the section "Optical Characteristics"
- Measured temperature: 25° C unless specified
- Measurement system: See the chart below.
- Measurement point: At the center of the screen.





## 2. Test Method

Notice	Item	Test method	Measuring instrument	Remark
1	Response time	<p>Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white.</p> 	LCD7200	<p>Black display [Data]=00h White display [Data]=3Fh TON Rise time TOFF Fall time</p>
2	Contrast ratio	<p>Measure maximum luminance Y1([Data]=3Fh) and minimum luminance Y2([Data]=00h) at the center of the screen by displaying raster or window pattern. Then calculate the ratio between these two values.</p> <p>Contrast ratio = Y1/Y2</p> <p>Diameter of measuring point: 8mmφ(CS1000)</p> <p>Diameter of measuring point: 3mmφ(LCD7200)</p>	CS1000 LCD7200	Backlight ON Backlight OFF
3	Viewing angle Horizontalθ Verticalφ	Move the luminance meter from right to left and up and down and determine the angles where contrast ratio is 10.	EZcontrast160D	
5	White chromaticity	<p>Measure chromaticity coordinates x and y of CIE1931 colorimetric system at [Data] = 3Fh</p> <p>Color matching faction: 2°view</p>	CS1000	
6	Burn-in	Visually check burn-in image on the screen after 2 hours of "window display" ([Data]=3Fh/00h).		At optimized VCOMDC
7	Center brightness	Measure the brightness at the center of the screen.	CS1000	
8	Brightness distribution	<p>(Brightness distribution) = 100 x B/A %</p> <p>A : max. brightness of the 9 points</p> <p>B : min. brightness of the 9 points</p>	CS1000	